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Low power & Area efficient Carry Select Adder using CMOS Technology

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Abstract - Adders are one of the extensively used digital components in digital integrated circuit design. The basic operation is addition which is used in almost all computational systems. Hence, the efficient implementation and design of arithmetic units needs the binary adder structures to be implemented in an equally efficient manner .A ripple carry adder has smaller area and it has also got less speed. A carry look ahead adder is faster though its area requirements are quite high. BEC Efficient Novel carry select adder proposed here actually provides good compromise between cost and performance and thereby establish a proper trade-off between time and area complexities. In the proposed work Tanner EDA tool is used for the designing of all adders containing Ripple carry adder, Binary to Excess One Convertor and Multiplexers.

Key Words: Carry Save Adder, Carry Select Adder, Ripple Carry Adder, and Binary to Excess one Converter, Square root Carry Select Adder, and Very Large Scale Integrated Circuits for Hardware Description Language.

I. INTRODUCTION

In the upcoming years, the rising demand for high-speed arithmetic units in micro-processors, image processing units and DSP chips has cleared the path for development of high-speed adders as addition is an requisite operation in almost every arithmetic unit and also it acts as the basic building block for synthesis of all other arithmetic computations. To increase convenience of systems and battery life, area and power are the critical factors of concern. Even in servers and personal computers (PC), power dissipation is a key design parameter. In today's situation, design of area efficient and power efficient high speed logic systems are the one of the decisive areas of research in VLSI design. In digital adders, the speed of addition is restricted by the time required for the carry to propagate through the adder. In the present scenario, there is a need that computations should be performed using low power and an area efficient circuit that must operate at greater speed which is reachable with lesser delay because of which the efficient adder implementations becomes an inevitability. Depending on the parameters required such as area, delay and power consumption, several adders can be implemented which are been proposed. In this project, qualitative evaluations of the classified binary adder architectures are given. CMOS design of Ripple Carry Adders, Carry Select Adders and Carry Look ahead adders is needed to emphasize the common performance properties which belong to their classes. In the following section, we give a brief description of the studied adder architectures. The leading class consists of the very slow ripple carry adder with the smallest area. In the second class, the carry skip, carry select adders with multiple level have small area requirements and short computation times. From the third class, the carry look Ahead adders and from the fourth class, the parallel prefix adder represents the fastest addition schemes with the largest area complexities.

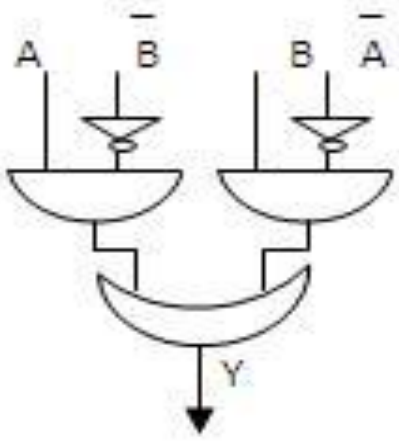


Fig 1: Delay and area Evaluation of XOR

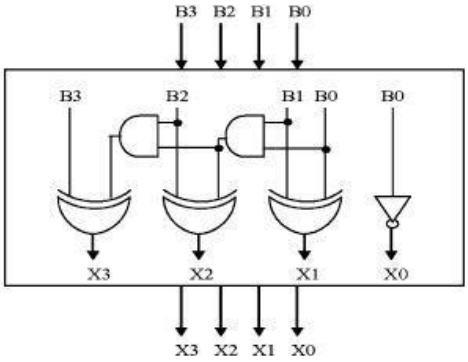


Fig 2: 4-bit BEC.

Table-I

DELAY AND AREA COUNT OF THE BASIC BLOCKS OF CSA, RCA AND CSLA

Adder block	Delay(ns)	Area
X-OR	3	5
2:1 Mux	3	4
Half Adder	3	6
Full Adder	6	13

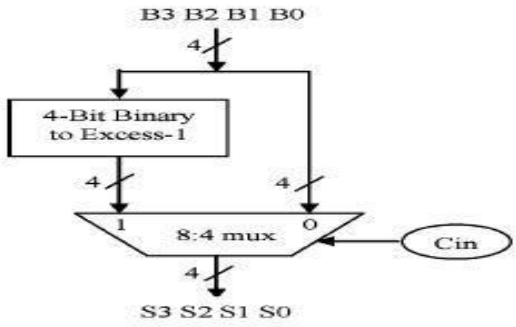


Fig 3: 4-bit BEC with 8:4 mux.

II. 2.1 CARRY SAVE ADDER

A carry save adder is one type of digital adder which is used in computer architecture circuits for the computations of the sum of three or more *n*-bit numbers in binary. It is different from other digital adders in that it outputs the two numbers of the same dimensions as that of the inputs, one of which is a sequence of partial sum bits and another which is a sequence of carry bits. The carry save unit consists of *n* full adders, each one of which performs a single sum and carry bit whose base completely depends on the corresponding bits of the three input numbers. For Example :- If Given there are three *n* - bit numbers **a**, **b**, and **c** it produces a partial sum $\mathbf{Ps_i}$ and a shift-carry $\mathbf{Sc_i}$ When adding together three or more numbers, using a carry save adders followed by a ripple carry adder which is faster than using two ripple carry adders. This is because a ripple carry adder cannot compute a sum bit without waiting for the previous carry bit to be produced, and thus has a delay equal to that of *n* full adders. A carry save adder, however produces all of its output values in parallel, and thus has the same delay as a single full-adder. Thus the total computation time (in units of full-adder delay time) for a carry save adder plus a ripple carry adder is $n + 1$, whereas for two ripple carry adders it would be $2n$.

2.2 CARRY SELECT ADDER USING RIPPLE CARRY ADDER

All the arithmetic operations such as addition, subtraction, multiplication, division are the basic operations to be implemented in digital computers using basic logic gates for eg. AND, OR, NOT, NOR, NAND, EX-OR, EX-NOR etc. Among all the arithmetic operations if we can implement addition then it is easy to perform multiplication, subtraction and division .Half Adders can be used to add two one bit binary numbers. It is also possible to create a logical circuit using multiple full adders to add N-bit binary numbers. Each full adder inputs Carry input which is the Carry output of the previous adder. This kind of adder is **a** Ripple Carry Adder, since each carry bit "ripples" to the next full adder. The first full adder may be replaced by a half adder. The block diagram of 16-bit Ripple Carry Adder is shown here below-

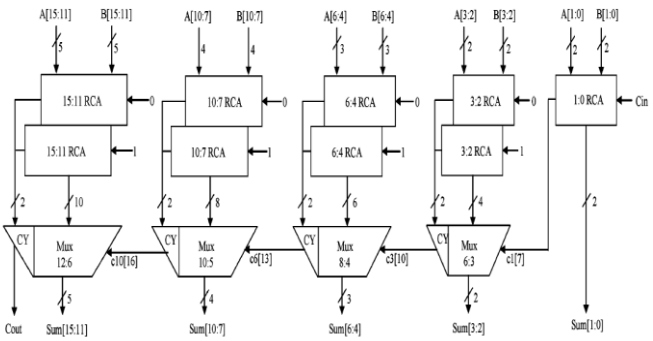


Fig 4: - Regular 16 bit Carry Select Adder using RCA

III. DELAY METHODOLOGY of CSA,CSLA USING RIPPLE CARRY ADDERS AND CSLA USING BEC- 1

Delay and Area Evaluation methodology of CSA, CSLA using ripple carry adder and CSLA using BEC-1 is shown in below table. In 16-bit CSA the area is increased as compared to regular CSLA and modified CSLA modified CSLA. In 16-bit SQRT CSLA moderate area is required as compared to CSA and CSLA using RCA. Delay is reduced by using 16-bit SQRT CSLA as compared to 16-bit CSLA using RCA .The n 16-bit SQRT CSLA moderate area is required as compared to CSA and CSLA using RCA. Delay is reduced by using 16-bit SQRT CSLA as compared to 16-bit CSLA using RCA .The comparative values of Voltage, Static Current and power shows that the number of Multiplexers required will be same but the gate counts of the overall circuit will get reduced due to Binary to excess-1 convertor as it requires less number of gates.

Table -1: Comparison In terms of Delay/Area

Sr. No	PARAMETER	16-Bit CSLA using RCA	Modified 16-Bit CSLA using BEC
1	Voltage (Volt)	0.8	0.8
2	Static Current(Amp.)	2.45u	7.745 n
3	Power(Watt)	1.963 u	6.196 n

IV. RESULT

The implemented Design of 16-bit SQRT CSLA has been simulated using Tanner. The 16-bit CSLA adder are designed and simulated using Tanner and the results are compared with CSA and Carry Select Adder using RCA. The modified CSLA structure decreases the power consumption & Area. The area can be reduced by using BEC structure instead of RCA.

Fig -1: Simulation Result of 5- Bit BEC

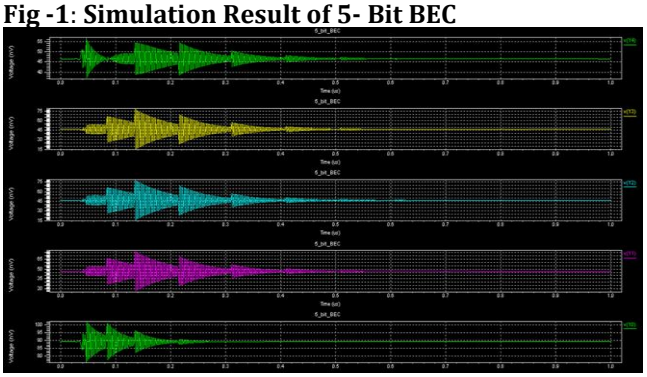
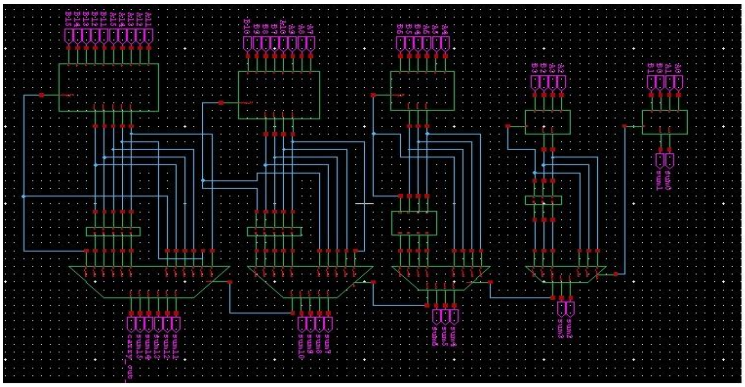


Fig -2: Design of 16-bit SQRT CSLA using BEC



V.CONCLUSIONS

In this paper a proposed simple approach is shown that how to reduce area and delay of Square Root Carry Select Adder using Binary to Excess one architecture. The Ripple Carry Adder with Binary to Excess one Converter in the structure is a great advantage for reducing the number of gates. The result as shown in comparison table states that the modified 16-bit Square Root Carry Select Adder has a slightly large area for lower order bit which reduces for higher order bit and also delay is reduced to a great extent. Thus the result shows that using modified method the area and delay will decrease so it is a good alternative for adder implementations in many data processors.

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