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A Review on Design and Simulation of Extended Golay Decoder

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Abstract - *An efficient implementation in the area of field programmable gate array (FPGA) by using both binary Golay code (G_{23}) and extended binary Golay (G_{24}) can be done with the help of number of encoding scheme such as Hamming code, block code, Turbo codes, CRC-cyclic redundancy check-based etc. High speed with low-latency and less complexity architecture is the main concern area at the time of working on FPGA. To remove the complexity and for the fulfillment of the requirement of the system this paper present a review on number of scholars and on the bases of that a new scheme is proposed in future for FPGA using both binary Golay code (G_{23}) and extended binary Golay (G_{24}).*

Key Words: FPGA, CRC cyclic redundancy check, Golay code, Extended Golay code, Encoding, Decoding, Hardware optimization.

1.INTRODUCTION

In wireless communication system the signal travel in the environment will be diffracted, scattered, reflected and refracted because of the obstacle presents in the environment which means the system is in a non-Line-of-sight (NLOS) environment. However the signal is distorted and there may be error present in the information when passing through different features in the course of transmission. So there is a concern how to reduce the error probability of digital signal in real time communication system. The reason for these signal distortion is multipath interference and noise that are received at the time of transmission and this can be overcome by using channel coding technology. In view of the fact that this technology must add some redundancy bits to the original data at the time of transmission the channel coding must add excess bits to the original data in transmitting called parity bit or redundant bits, as a result of that we can detect and correct the error bits of signal. By appending the additional bit to the data as parity this will reduce the energy of the symbol of the received signal as a result of that receivers symbol error rate increase. But if more error bits can be corrected to reimburse for the symbol error rate that increases by the decreasing the energy of the symbol, the bit error rate of the whole received signal still can be reduced. By reducing the power efficiency Eb/N0 of the received digital signal after decoding will be requirement for achieving the same bit error rate. The symbol error rate of the received signal can be reduce by avoiding the more addition of parity bits for that a threshold value of signal to noise ratio is to be set and to achieve the coding gain, this the signal-to-noise (SNR) of the received signal Eb/N0 must reach to that threshold. The decoding mechanism is not responsible for this reduction in the symbol rate and cannot compensate for this loss. Consequently, the selection of coding rate is very important; or we can say that for different systems depends on the specification requirement different encoding modes and different coding rates should be adopted. The decoding capability of the channel code is influence by the coding rate that determined by the number of information bits and parity-bits.

Channel coding in a wireless communication channel environment is a technology to improve the bit error rate of signal in transmission. To achieve the lower bit rate at the same transmission power the bandwidth is modified the excess part of the bandwidth is taken out. Alternatively, the quality required for the communication can be obtained at lower transmitted power; however we achieve the coding gain of the channel code. These can be fulfilling only when we achieved the Eb/N0 threshold of received signal are reached. The most frequent problem in wireless channel environment is the interference and noises from different environments, obstacles and user moving. Consequently, problems in coding is encountered due to the occurrence of the burst errors to solve this problem block interleaving is one of the most appropriate method to break up the burst error in to discontinuous random error to bring the capability of channel coding to correct errors. One more complexity encountered at the time of coding and decoding that addition of more redundant bits increase the system complexity and the need of storing that bits is also become complicated ,requirement of large memory, buffers, complex software and hardware design is become very complicated. There are five sections in this paper. One of the best possible ways to present the coder and decoder and a new approach to remove the errors is use Golay code to encrypt the data the central idea of using this code is to restrained the amount of errors as much as possible. For that addition of the redundancy bits to the messages is one of the best idea through which facilitate to find out or correct the errors that may have occurred. This paper proposed a specific type of error-correcting codes, Golay codes (23) and the extended Golay code (G24). Three steps to transfer the information, a channel transmit, and a receiver. At the time of transmission

the information is changed to noise so to avoid this condition use error correction codes.

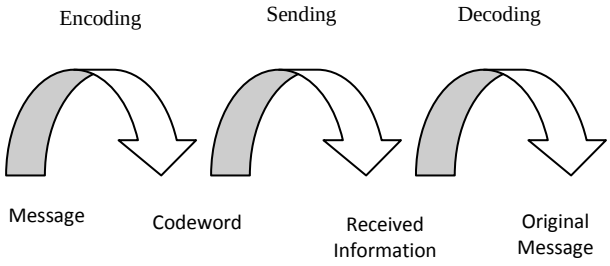

Fig -1: Communication System Process Steps

Fig. 1 show that a message is encoded into a codeword, it is sent to the receiver through a channel, in this channel the opportunity exists that errors occur, and the receiver tries to obtain the original message by decoding the word. The transmission of message depends on what we have received and what is send. Some important properties that give a detailed description of the extended Golay are described as follows:

1) First property shows that a message m of length k out of some finite field F generates sequence of k symbols, so m = (m1: mk) belongs to F^k. Then an n-code Cover a finite field F is a set of vectors in F^n, where n ≤ k. Since we will be commerce with a binary code only, we will assume codes are binary from now on.
2) Second property says that the error of p probability occurs only when 0 is received when 1 was sent, or 1 is received when 0 was sent.
3) Third property says that the function F^n is a non-zero elements and hamming weight of a vector belongs to that function.
4) Fourth property says that the humming distance of two vectors belongs to a function F^n is the number of place where they differ. The idea is that an n-code C is a strict subset of F^n in which we want the Hamming distance between any two vectors to be as large as possible. Therefore, the minimum Hamming distance is an important characteristic of the code.
5) Fifth property says that the minimum Hamming distance d of a code C is defined as d = min {dist(x, y) I x, y belongs to C} where c is the code.

Golay Code Encoder Algorithm

The following steps are used for the encoding procedure that is enlisted as follows:

1) For check bits generation a characteristic polynomial is preferred.
2) Long division method is used to contribute 'M' bit data with the characteristic polynomial. So, 11 zeros are appended to the right of data message M.
3) The check bits for G (23) are obtain by the most significant bit (MSB) resulted at the end of the division operation.
4) The encoded Golay code (23, 12, 7) codeword are obtained by Appending check bits with the message.
5) For conversion of binary Golay code into extended binary Golay code (24, 12, 8) a parity bit is added. If the weight of binary Golay code is odd, then parity bit 1 is appended, otherwise 0 is appended.

The Golay code encoding is explained using example in fig. 2

Data (12-bit)	Appended zeros	Operation
101000100111	00000000000	
101011100011		... 12-bit xor
0000110001000000		... 1-bit shift
101011100011		... 12-bit xor
0110101000110		... 1-bit shift
101011100011		... 12-bit xor
0111101001010		... 1-bit shift
101011100011		... 12-bit xor
0101101010010		... 1-bit shift
101011100011		... 12-bit xor
000110110001000		... 1-bit shift
101011100011		... 12-bit xor
0111011010110		... 1-bit shift
101011100011		... 12-bit xor
010000110101		
<Check-bits>		

Fig 2 Long Division of Data for Check bits generation

Golay Code Decoder Algorithm

The following steps are used for the decoding procedure that is enlisted as follows:

1) For the received codeword 'W' and matrix 'H', where H = [I / B] Compute the Syndrome 'S'.
2) Error vector, E = [S, 0], If weight of 'S' is less than or equal to 3, i.e., wt(S) ≤ 3.
3) If wt(S+B*i*) ≤ 2, then E = [S+B*i*, I*i*]. Where I*i* represents i^{th} row of the identity matrix I.
4) The second syndrome SB can be computed
5) If wt(SB) ≤ 3, then E = [0, SB]
6) If wt(SB+B*i*) ≤ 2, then E = [I*i*, S+B*i*]

If E is still not determined then received data is required to be retransmitted.

The first section presents an introduction about the problem occurrence at the time of transmission and the reason why the occur and how we can resolve it to achieve high performance system. The second section is the literature review that presents the work or other scholars. Third section is conclusion and forth is Acknowledgment the last section is about the reference paper.

2. LITERATURE REVIEW

Reference [1] is an IEEE Transaction paper which presents an efficient hardware implementation of encoder and decoder for both prototype binary Golay code (G23), extended binary Golay code (G24) based on CRC (Cyclic Redundancy Check) encoding scheme.Virtex-4 FPGA is used to design high speed with low latency architecture. This proposed method has various applications in the field of high speed communication links, photo spectroscopy, and ultrasonography. Reference [2] is a paper written by Mr. Golay himself. This paper proposed lossless binary coding scheme to assure the reception of the correct data. To overcome the problem of power loss which is introduced by ternary coding scheme, a 23 binary symbols is used which yields the power saving one and a half db for omitting probability of errors and this code is called Golay code. And another code is also introduced by him called extended Golay code but it is not that much power efficient it yields the power saving up to 3 db. Reference [3] this paper presents the outperformance of the extended Golay code under the hard decision decoding. And compare the performance of the binary Golay code and extended binary Golay code under the ML (maximum likelihood) conditions. Reference [4] presents the overview about the Golay codes and their properties. (G11) is ternary Golay code and (G23) binary cyclic code. Reference [5] presents GF (2m) Galois field encoder & decoder and its verification on FPGA using the NIST chosen irreducible polynomial. Software used to do this is Xilinx ModelSim 10.0 that simulated complete verification of multiplication& implemented on FPGA. The paper presents simple circuit and performs high speed operation by increases security during communication dialogue and decreasing the number of logic gates. Reference [6] proposed a simplified soft decoding algorithm to correct up to four errors for extended binary Golay code .The results obtained by this method shows the less complex calculation were required with this method and also work on the efficiency hardware implementation on FPGA platform. And presents the detailed architecture of soft decoder and the results is also compared with the other algorithms in terms of power gain, cost, and hardware complexity. Reference [7] proposed a method to construct the binary Golay code (24, 12, 8) by using two array codes involving four component codes. Two of them are simple linear block codes and other two are symmetric code and its extended version. Reference [8] presents overview on Golay Complementary Sequence. These sequences are introduced by Marcel Golay in the perspective of infrared spectrometry and also give the properties and applications in different fields. Reference [9] proposed a new algorithm to decode the binary systematic (23, 12, 7) and (14, 21, 9) QR codes. The proposed algorithm by using lookup table directly determines the error locations without the operation of multiplication over a finite field. The reason of using the FLTD is the CPU time is half of the LTD algorithm. In terms of both speed and memory requirement in real time system FLTD algorithm is better approach as compare to the existing ones. Reference [10] proposed symbol –by –symbol soft in/ soft out APP decoding algorithm for the Golay code. This decoding algorithm is suitable for convolution codes and block code with simple trellis structure. Reference [11] proposed block product turbo code (BPTC) and simulated its efficiency. The proposed method used hamming (15, 11) and hamming (13,9) block channel code in combination to construct a BPSK modulation .This combination gives better results and robust against BPSK Golay code and MSK Golay. Application of the proposed algorithm is in the wireless communication system. Reference [12] proposed a new scheme which is reversing of the conventional Golay code (24, 12, 8) which maps 24- bit vector into 12 bits message words. In this approach each object is represented by 24 bit vector at the same time we consider 1 bit probability distortion through bit modification. Consequently, this work proposed a hash table of 4096 entries that is fault-tolerant. This allows organizing a direct retrieval of a neighborhood of 24-bit vectors with two or possibly more mismatches. A retrieval capability of the proposed system and the expected hash distribution is obtained by the simulation experiments. Reference [13] proposed a methodology of constructing a sequence of phase-coded waveform for which ambiguity function is free of ranges side lobes along doper shift. The problem arises with Golay code is that it has ideal ambiguity along zero Doppler-axis but are sensitive to nonzero Doppler shifts. And the application of pulse coded waveform is in the area or communication using radar. Reference [14] proposed an error correction Golay code for clustering tremendous amount of Big data Streams by using error correction Golay codes and this approach is used in the field where the requirement to accumulate multidimensional data. In Reference [15] the proposed methodology fulfill the requirement reducing the peak to average ratio (PTAR) with the help of special Fractional Fourier Transform (FRFT) followed to the low complicity Golay sequence coder in order to provide optimal de-correlation between signal and noise. To achieve the requirement of low complexity, low bit error rate and peak to average power ratio. Reference [16] proposed an algorithm for the hardware implementation of (24, 12, 8) Golay code in FPGA (Field programmable gate array) based system. To remove the complexity of arithmetic operations this arises in the existing algorithm. The proposed algorithm chooses the absolute value rather than bit error probability to obtained better results as compared to the existing algorithms. Reference [17] proposes a new algorithm to fulfill the requirement of faster decoding for the Gosset Lattice, Golay code and Leech Lattice. The proposed design introduced two approaches to first when charge in of length n and taking soft decoding algorithm at an arbitrary point R^n in to the nearest code word and second a decoding algorithm for a lattice A in R^n changes an arbitral point of R^n into a closest lattice point. Reference [18] proposed an efficient soft-decision decoder of the (23, 12, 7) binary Golay code up to the four errors and almost all patterns of three errors and all fewer random error can be corrected with the help of proposed algorithm.

3. CONCLUSIONS

This paper presents a review on different research work presented in the field FPGA based speed optimization bust

error reduction etc. Different coding and decoding methods were introduced in the reference papers to control the errors and for the speed optimization. Here, the main aim is to present systems which remove the complexity of system on fulfillment the requirement of high speed application and low latency data. So that a new scheme is proposed in future for FPGA using both binary Golay code (G_{23}) and extended binary Golay (G_{24}).

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