Design of Low Power Low Voltage Circuit using CMOS Ternary Logic

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Abstract— *Binary logic and devices have been in use since inception with advancement and technology and millennium gate design era. Now binary logic has become tedious and complicated. For this purpose the low power and low voltage arithmetic and logic circuit designed. In this paper we will presents the design and performance of Arithmetic and Logic circuit using Ternary logic and CMOS design styles. The design is targeted for the 45nm CMOS technology. Design tool for simulation will be MICROWIND 3.1 software and DSCH tool. We will estimate area, power and delay and the design of arithmetic circuit with optimized number of transistors as compared to binary circuit.*

***Index Terms*—Logic, Ternary, CMOS, Arithmetic Circuit, Low Power, Low Voltage.**

I. INTRODUCTION

In new technologies, most delay and power occurs in the connection between gates. When designing a function using Ternary logic or Multiple valued logic, need less gates, which implies less number of connections and the less delay. The ternary logic or trivalent logic is one of logical calculi in which there are more than two possible truth value. But Logical calculi are bivalent. There are only true and false possible values for any proposition. Two value and three value logic i.e. (True, false and intermediate) proposed by first author Lukasiewiczs. In this technology more than one or two value logic is implementing. Ternary logic means more than two truth value (0,1) logic i.e. n-value logic for n > 2. Here we implement three truth value logic i.e. (0,1,2) i.e. 2 for true, 1 for intermediate and 0 for false.

There are two modes i.e. current mode and voltage mode, where MVL is implemented. In current mode, in terms of output current MVL states are defined, which is an integral multiple of reference current and in voltage mode, MVL states are in terms of distinct voltage levels. In voltage mode operation of the circuit three distinct logic levels are defined in terms of voltage i.e. Low voltage level corresponds to logical state 0; intermediate to logical state 1; high to logical state 2 respectively.

- TERNARY LOGIC SYSTEMS

In this section, ternary logic system is described. The system includes a set of logic gate operators. The circuits can be designed using them. As discussed earlier ternary logic offers significant advantages in development. It is used to design entry method for our planned project.

- TERNARY LOGIC GATES

In ternary logic system, logic levels ranges from 0 to 2 as against 0 and 1 in binary logic. The logic systems uses logic gates and their operations is known as operators. The gates and operators can be interchangeably used. The following ternary gates/operators are in use and have been considered in our project.

1. NOT GATE – A NOT gate have one input and produce one output in ternary algebra. These gates are known as fundamental operator. Truth table gives the output 0; in case of when input is 2. Gives output 1; in case of input is 1. And when output is 2; then input would be 0. Their truth table and symbolic representation given below.

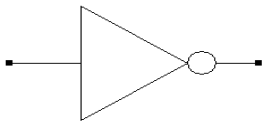


Fig-1: Ternary NOT Gate

Table-1: Ternary NOT Gate Truth Table

Operand	A	0	1	2
Output	$\bar{A}$	2	1	0

2. NAND GATE - A NAND gate have two inputs and produce one output in ternary algebra. These gates are known as a functional operator. Truth table gives output 2; in case of when input is 00. Gives output 2; in case input is 01. Gives output 2; in case input is 02, respectively. Their truth table and symbolic representation given below.

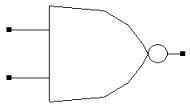


Fig-2: Ternary NAND Gate
Table- 2: Ternary NAND Gate Truth Table

Operand	A	0	1	2	0	1	2	0	1	2
	B	0	0	0	1	1	1	2	2	2
Output	$\overline{AB}$	2	2	2	2	1	1	2	1	0

3. NOR GATE- A NOR gate have two inputs and produce one output in ternary algebra. These gates are known as a functional operator. Truth table gives output 2; in case when input is 00. Gives output 1; in case when input is 10. Gives output 0; when input is 02,and so on. Their truth table and symbolic representation given below.

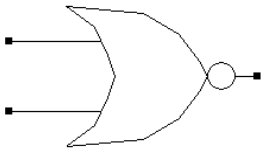


Fig-3: Ternary NOR Gate
Table-3: Ternary NOR Gate Truth Table

Operand	A	0	1	2	0	1	2	0	1	2
	B	0	0	0	1	1	1	2	2	2
Output	$\overline{A+B}$	2	1	0	1	1	0	0	0	0

II. RELATED WORK

1] A. P. Dhande, V.T.Ingole [10] This paper presents 3-valued R-S & D type of flip-flops is studied and described. To implement single clocked gates the minimum number of transistors are used. Less power consumption and speed of operation achieved.

2] Boris Svilicic, Antun Kras 2006[5] This paper examines issues related to the future development of CMOS technology. There is no alternative logic technology is evolving to threaten the CMOS dominance within cost/ performance products on the market today. CMOS provides lower power dissipation, higher packing densities and higher circuit speeds.

3] A.P.Dhande, R.C.Jaiswal, S.S.Dudam 2007 [9] This paper presents, the VHDL modeling and simulation of 1-bit multiplier circuit and T gate is described. The proposed work describes basic procedure & establishes VHDL as tool for simulation of ternary circuits and systems. To synthesis and to verify the performance of ternary logic circuits, the proposed simulator can be used.

4] Omid Hashemipour, Akbar Doostaregan, and Keivan Navi [4] 2010 In this paper, a low power and high performance Standard Ternary Inverter for CMOS technology has been proposed. Less power consumption can be achieved using MOS transistor and capacitor. Operation and performance of the proposed design has been examined and simulated by using Synopsys HSPICE tool.

5] R.K.Nagaria,S.S.Mishra and Adarsh Kumar Agrawal 2010[1] In this paper, author reviewed various design techniques for XOR-XNOR circuit. Evaluates & compares the performance of various design techniques of XOR-XNOR circuits based on delay, PDP, EDP etc. Very low power consumption and a very high speed performance can be achieved.

6] Kanchan S. Gorde 2010[2] This paper presents, design and simulation of ternary logic based arithmetic circuits is explained. At ±5V power supply voltage STI, PTI and NTI inverters have been designed for operation. Simulation have been carried out by using MICROWIMD and SPICE software.

7] Mariana Aguirre-Hernandez, Monico Linares- Aranda 2011 [7] In this paper author describes all the detail information regarding to design and performance comparison of full adder using alternative internal logic structure. Full-adder were built in combination with pass-transistor powerless or groundless logic styles and designed with a TSMC 0.18-m CMOS technology. From this paper we got information regarding to the problem occur during the design of full adder. Also we get the alternative structure which is used for designing adder.

8] Rajendra Kumar Nagaria, Sudarshan Tiwari, and Subodh Wairya 2011[11] This paper presents a comparative study of high-speed and low-voltage full adder circuits. Using hybrid-CMOS design style with pass transistor a new full adders designed are presented in this paper that targets low PDP. An alternative internal logic structure for designing full adder cells is introduced.

9] M.B. Srinivas, Chetan Vudadha, Sreehari V 2012[3] This paper presents a multiplexer based methodology for design of ternary logic circuits. CNFET based ternary and binary circuits are used to implement the proposed methodology. Simulations results indicate that the proposed 1-bit half adder has 27% less delay and 23% lower power delay product, when compared to the existing design. Existing as well as proposed design methodology, have been performed in HSPICE using the CNTFET model.

10] Bhavna Jharia, Priyanka Rathore 2014[6] This paper presents comparison of different full adder circuits which are made of various logic styles. On the basis of comparison of different full adder circuits which are made of various logic styles and suggests the best technique of designing on the basis of performance. Power consumption and area parameters are considered.

11] Shruti Tiwari and Dwejendra Arya 2014[8] This paper presents modeling and simulation of low power 1 bit CMOS full adder cells. The highest speed of operation i.e. minimum delay is achieved by circuit. Very low leakage power consumption, the speed of operation is modest i.e. intermediate delay is achieved by the circuit.

III. PROPOSED WORK

Here we propose Ternary implementation of arithmetic and logical operations such as comparator, NOT gate, NAND gate and NOR gate etc using ternary input and obtained the ternary output using CMOS technology.

- There are some methods for implementation of arithmetic and logical operation.

1) BINARY LOGIC
2) TERNARY LOGIC
3) QUATERNARY LOGIC

But we perform the different operations only by using Ternary logic only.

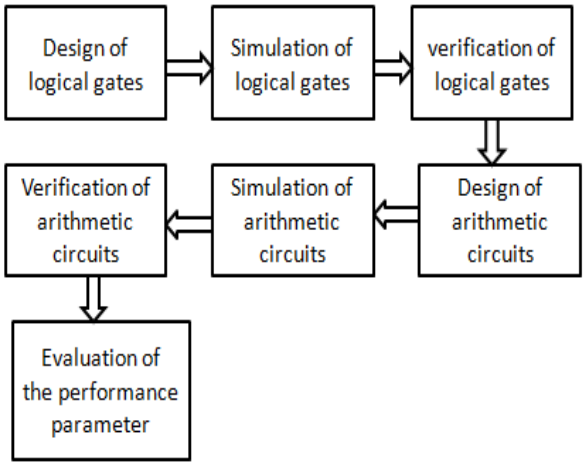


Fig-4: Proposed System Design Flow

Above figure shows Stepwise working of the proposed approach. In this model, first we have to design logic gates. Then by using this logic gates arithmetic circuits are design. Performance of both models is evaluated on the basis of power consumption, area/ size, time etc.

The detailed working of the proposed approach is as follows:

1.Implementation of Ternary for NOT gate/ Inverter

A ternary NOT gate or ternary inverter, have one input and produced one output. Fig.5 explains the basic inverter or NOT gate. If input is 0 then output is 1 and if input is 1 then output is 0. In truth Table.4 in and out is input and output respectively.

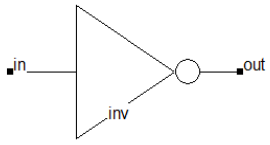


Fig-5: Basic Inverter

Table-4: Truth Table of Binary Inverter

in	out
0	1
1	0

Fig.6 explains the basic schematic of Inverter using pmos and nmos transistor in DSCH tool. In which if input 0 is applied then transistor pmos become 1 i.e. connected to Vdd and transistor nmos become 0 i.e. connected to ground or Vss, at the output we get 1. Likewise if input 1 is applied then transistor nmos become 1 and transistor pmos become 0, at output we get 0.

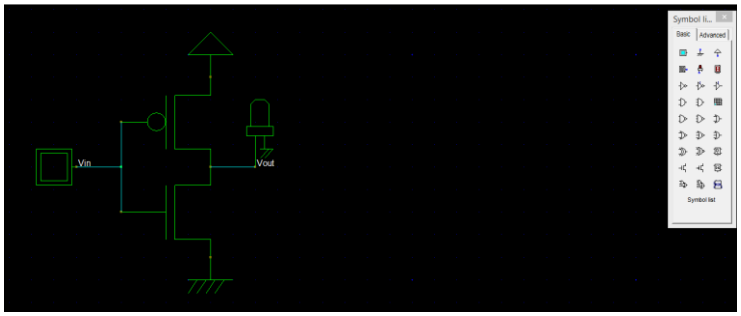


Fig-6: Basic Schematic of Inverter

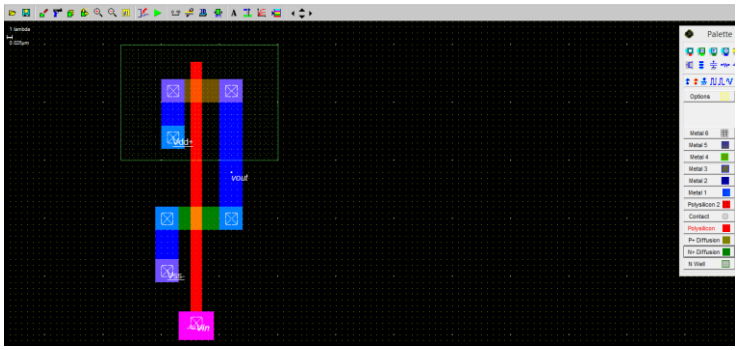


Fig-7: Layout of Inverter

Fig.7 explains the layout of Inverter in MICROWIND 3.1 software. In ternary logic three values can be applied as an input i.e. 0, 1 or 2 as discussed earlier. By applying ternary logic, output Vout is 2; if in case input Vin is 0. Output Vout is 1; if input Vin is 1. And output Vout is 0; if input Vin is 2. Table.5 explains the truth table of ternary inverter, where in and out are ternary input and output respectively.

Table-5: Truth Table of Ternary Inverter

Vin	Vout
0	2
1	1
2	0

2.Implementation of Ternary for NAND gate

A NAND gate have two inputs and produce one output. It is simply inversion of AND gate. Basic principle of NAND is, if

both the input is high then output is low; otherwise output is high. Fig.8 explains the basic NAND gate. Table..6 is truth table of NAND gate where A0 and A1 are inputs and Vought is output respectively.

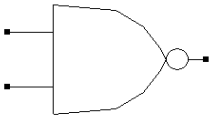


Fig-8: Basic NAND Gate

Table-6: Truth Table of Binary NAND Gate

A0	A1	Vout
0	0	1
0	1	1
1	0	1
1	1	0

Fig.9 explains the basic schematic of NAND gate using pmos and nmos transistor. In which if input A0 =0 and A1= 0 is applied then both transistor pmos become 1 i.e. connected to Vdd and both transistor nmos become 0 i.e. connected to ground or Vss, at the output we get 1. Likewise if input A0=1 and A1=1 is applied then both transistor nmos become 1 and both transistor pmos become 0, at output we get 0 and so on.

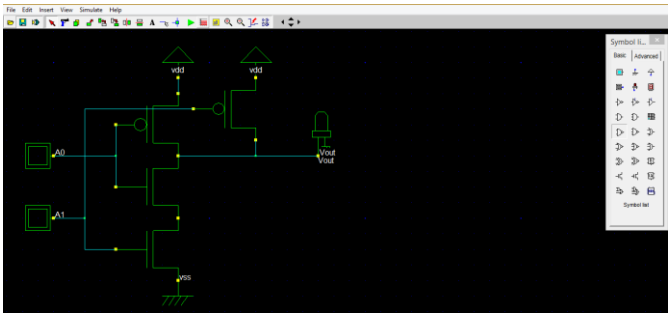


Fig-9: Basic Schematic of NAND Gate

Fig.10 explains the layout of NAND gate. In ternary logic three values can be applied as an input i.e. 0, 1 or 2. By applying ternary logic, output Vout is 2; if in case both input A0 and A1 is 0. Output Vout is 1; if both input A0 and A1 is 1. And output Vout is 0; if both input A0 and A1 is 2 and so on. Table.7 explains the truth table of ternary NAND gate, where A0 and A1 are ternary input and Vout is output respectively.

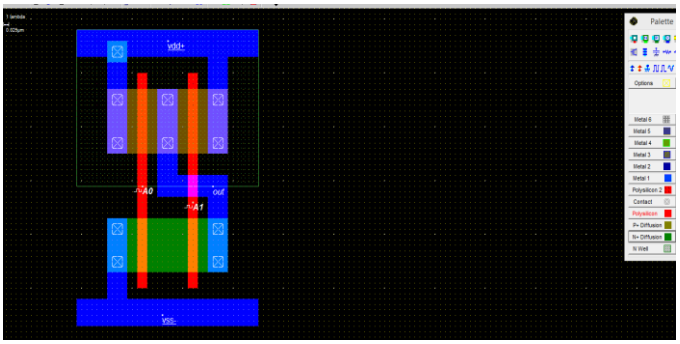


Fig-10: Layout of NAND Gate

Table-7: Truth Table of Ternary NAND Gate

A0	A1	Vout
0	0	2
0	1	2
0	2	2
1	0	2
1	1	1
1	2	1
2	0	2
2	1	1
2	2	0

3.Implementation of Ternary for NOR gate

A NOR gate have two inputs and produce one output. It is simply inversion of OR gate. Basic principle of NOR is, if both the input is same then output is high; otherwise output is low. Fig.11 explains the basic NOR gate. Table.8 is truth table of NOR gate where A0 and A1 are inputs and Vout is output respectively.

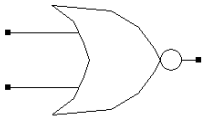


Fig-11: Basic NOR Gate

Table -8: Truth Table of Binary NOR Gate

A0	A1	Vout
0	0	1
0	1	0
1	0	0
1	1	0

Fig.12 explains the basic schematic of NOR gate using pmos and nmos transistor. In which if input A0=0 and A1= 0 is applied then both transistor pmos become 1 i.e. connected to Vdd and both transistor nmos become 0 i.e. connected to ground or Vss, at the output we get 1. Likewise if input A0=1 and A1=1 is applied then both transistor nmos become 1 and both transistor pmos become 0, at output we get 0 and so on.

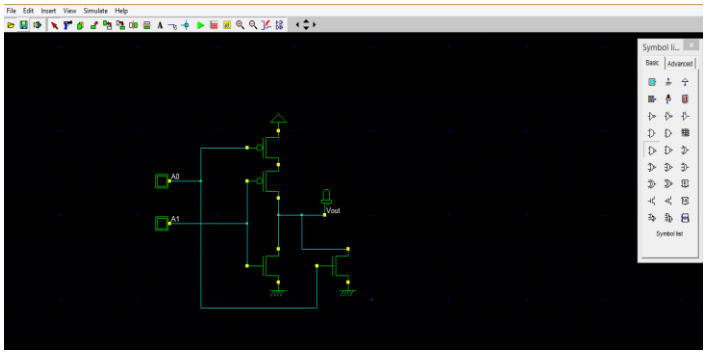


Fig-12: Basic Schematic of NOR Gate

Fig.13 explains the layout of NOR gate. In ternary logic three values can be applied as an input i.e. 0, 1 or 2. By applying ternary logic, output Vout is 2; if in case both input A0 and A1 is 0. Output Vout is 1; if both input A0 and A1 is 1. And output Vout is 0; if both input A0 and A1 is 2 and so on. Table.9 explains the truth table of ternary NOR gate, where A0 and A1 are ternary input and Vout is output respectively.

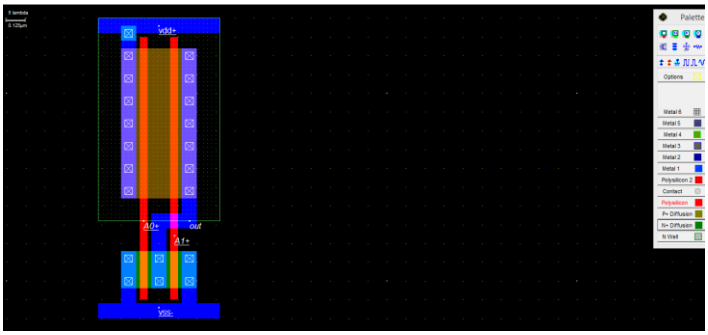


Fig-13: Layout of NOR Gate

Table-9: Truth Table of Ternary NOR Gate

A0	A1	Vout
0	0	2
0	1	1
0	2	0
1	0	1
1	1	1
1	2	0
2	0	0
2	1	0
2	2	0

4.Implementation of Ternary for Comparator

Proposed comparator circuit is based on ternary comparator. Here comparator simply compares the two input and indicate that whether the inputs are equal, less or greater than another input. Fig.14 explains the basic schematic of comparator, where A and B are the two inputs of comparator and by applying all possible combinations of 0 & 1 it produced the output.

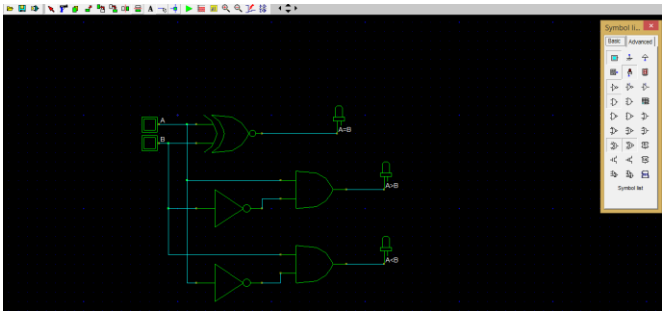


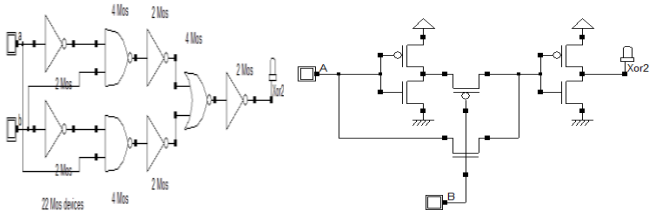
Fig-14: Basic Schematic of Comparator

Table 10 explains the truth table of comparator. When input A is 0 and B is 0 then at output we get A=B is 1. If in case A is 0 and B is 1 then at output A<B is 1. If in case A is 1 and B is 0 then A>B is 1 and at last if A is 1 and B is 1 then A=B is 1.

Table-10: Truth Table of Comparator

A	B	A=B	A>B	A<B
0	0	1	0	0
0	1	0	0	1
1	0	0	1	0
1	1	1	0	0

Comparator circuit consists of EX-NOR gate, inverter and AND gate as shown in fig.14 and total number of transistor required for comparator is 40. Shown in fig.14(a), for EX-OR gate total 22 transistor are required. By connecting it inverter it becomes EX-NOR gate and so that total required transistors are 24. By optimizing EX-OR gate only six transistor are used shown in fig.14(b) and hence for EX-NOR gate total 8 transistor are used.



(a) (b)

Fig.14(a) Optimized Schematic of EX-OR with 22 Transistors and (b) Optimized Schematic of EX-OR with 6 Transistors

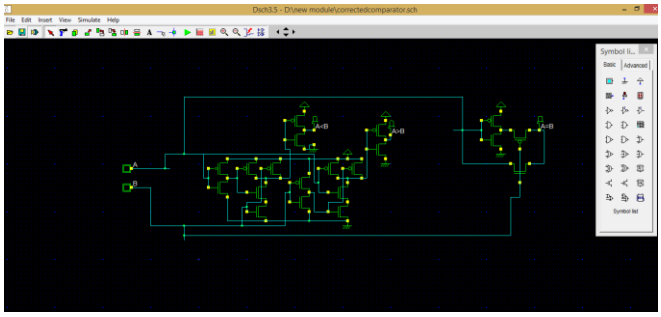


Fig-15: Optimized Schematic of Comparator

So conventional comparator required total 40 transistor. Optimization logic used here by replacing AND gate by NAND & NOT gate and optimized EX-OR gate is used with six transistors. Fig.15 explains the optimized schematic of comparator required total 24 transistor. By using the modified comparator we can save the 20 transistors with their power, energy and area.

Transistor Required For Simple Comparator	Transistor Required For Optimized Comparator
40 Transistor	20 Transistor

Fig.16 explains the layout of comparator. In ternary logic three values can be applied as an input i.e. 0, 1 or 2. By applying ternary logic, if input A is 0 and B is 0 then A=B is 2. In case if input A is 1 and B is 2 then A<B is 2. In case if input A is 2 and B is 1 then A>B is 2. If A is 2 and B is 2 then A=B is 2; and so on. Figure 4.6.2 explains truth table of Ternary comparator where A and B are inputs and A=B, A>B and A<B are outputs respectively.

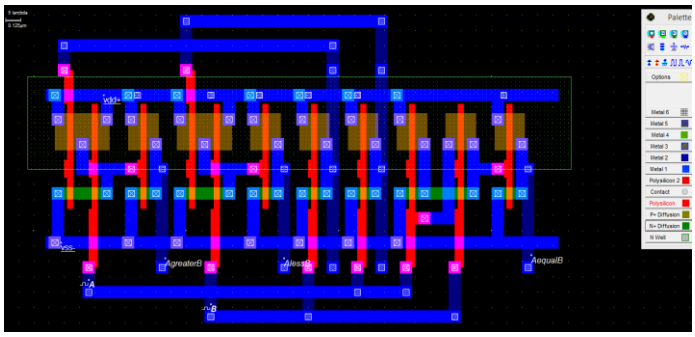


Fig-16: Layout of Comparator

Table-11: Truth Table of Ternary Comparator

A	B	A=B	A>B	A<B
0	0	2	0	0
0	1	0	0	2
0	2	0	0	2
1	0	0	2	0
1	1	2	0	0
1	2	0	0	2
2	0	0	2	0
2	1	0	2	0
2	2	2	0	0

IV. RESULTS & DISCUSSION

Simulation Results

The simulated results of implemented design of Basic gates and Arithmetic circuits are shown below. All the circuits are designed, simulated and the performance is evaluated based on power, delay, frequency and area/size etc. In waveform of ternary logic system shown below, there are three output levels i.e. logic 0, logic 1 means 0.6v, and logic 2 means 1.2v. Table 12 explains logic symbol of all circuits.

12.Table of Logic Symbols

Voltage Level	Logic Value	Considered Value
0	0	0v
½ Vdd	1	0.6v
Vdd	2	1.2v

A] Inverter

In fig.17, we can see the input and output waveform of the inverter. Minimum propagation delay of inverter is 10ps, from that we can calculate maximum frequency of inverter. Power consumption of inverter is 5 nw shown in fig.17. Consider one example of ternary inverter where, A is 2 that means 1.2v and B is 0v and output Vout is 0 shown in fig.18.

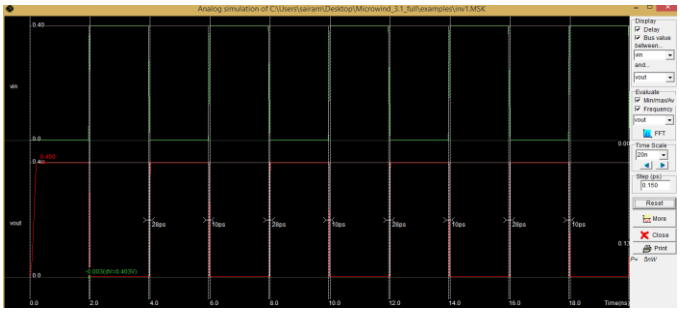


Fig-17: Input and Output Waveform of Inverter

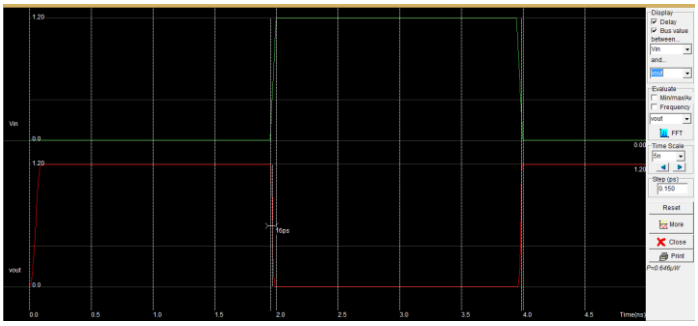


Fig-18: Input and Output Waveform of Ternary Inverter

B] NAND gate

In fig.19, we can see the input and output waveform of the NAND gate. Minimum propagation delay of NAND gate is 20ps. Power consumption of NAND gate is 0.052 uw shown in fig.19. Consider one example of ternary NAND Gate where, A is 1 and B is 1 and output Vout is 1 shown in fig.20.

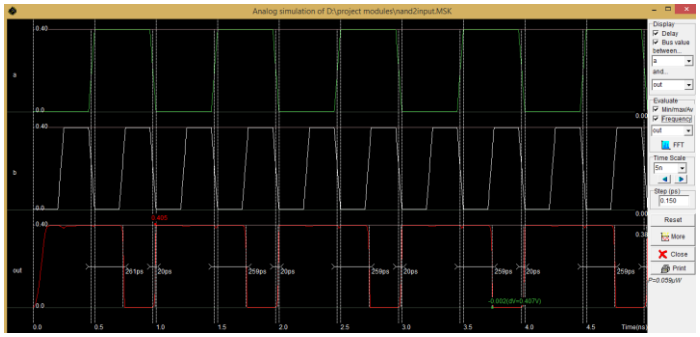


Fig-19: Input and Output Waveform of NAND Gate

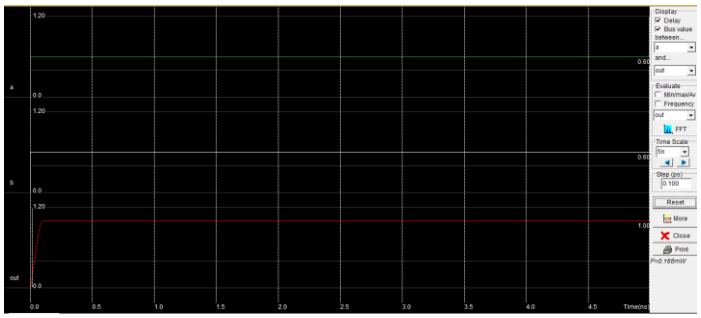


Fig-20: Input and Output Waveform of Ternary NAND Gate

C] NOR Gate

In fig.21, we can see the input and output waveform of the NOR gate. Minimum propagation delay of NOR gate is 20ps. Power consumption of NOR gate is 0.058 uw shown in fig.21. Consider one example of ternary NOR Gate where, A is 2 and B is 1 and output Vout is 0 shown in fig.22.

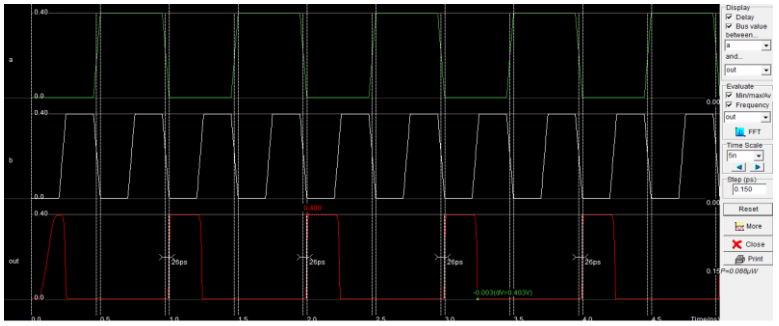


Fig-21: Input and Output Waveform of NOR Gate

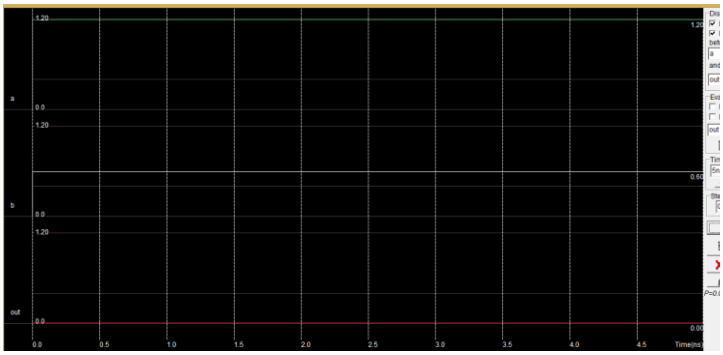


Fig-22: Input and Output Waveform of Ternary NOR Gate

D] Comparator

In fig.23, we can see the input and output waveform of the comparator. Minimum propagation delay of comparator is 0.034ns. Power consumption of comparator is 0.276 uw shown in fig.23. Consider one example of ternary comparator where, A is 1 and B is 2 and output A less B is 2 shown in fig.24.

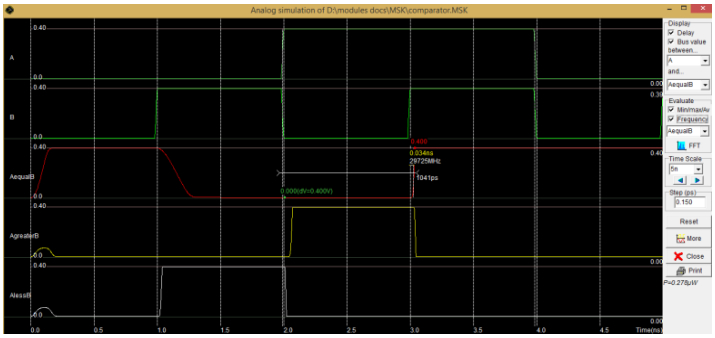


Fig-23: Input and Output Waveform of Comparator

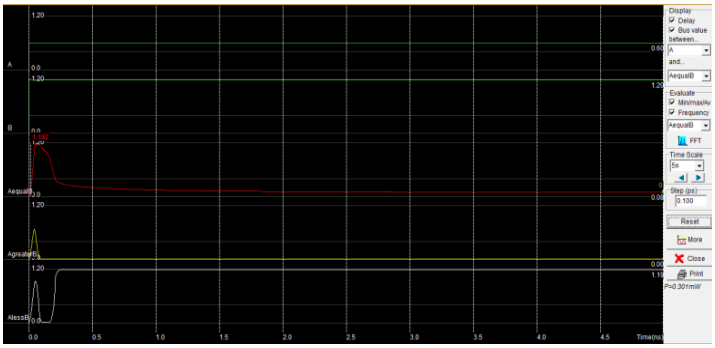


Fig-24: Input and Output Waveform of Ternary Comparator

Results and Discussion

Table.13 the summary of the proposed arithmetic and logic circuit in ternary logic system, evaluates the parameters based on number of transistor required, propagation delay, area, power and maximum frequency etc

Table-13: Summary of the Proposed Circuits

Circuit Parameters	Ternary Inverter	Ternary NAND gate	Ternary NOR gate	Ternary comparator
No. of transistor Required	2T	4T	4T	20T
Propagation Delay	10ps	20ps	20ps	0.034ns
Area	0.8606 um2	1.025 um2	1.6 um2	11.125 um2
Power	5nw	0.052uw	0.058 uw	0.276 uw
Maximum Frequency	1*10[11]Hz	5*10[10]Hz	5*10[10]Hz	2.94*10[10]Hz

Above all parameters are evaluated from the simulation waveforms in MICROWIND 3.1 software. Here maximum frequency calculated by using minimum propagation delay. For low power low voltage circuit application, circuit must have a minimum power consumption and maximum operating frequency. By using ternary logic, we get the minimum power consumption for all circuits with minimum delay and operated on a maximum frequency.

V. CONCLUSION

In this paper, we proposed a ternary logic circuit processing environment that it offers ease of ternary logic circuit design and development platform of ternary logic system. Looking to complexity of today's circuit, it is important that to develop circuit at higher than binary logic system so that complexity is reduced. So we designed ternary arithmetic and logical circuits like inverter, NOR gate, NAND gate, comparator etc with less number of transistors with minimum propagation delay. This MICROWIND 3.1/ DSCH tool simulation proves that ternary logic is better approach where the number of transistor count has been reduced in all proposed circuits and improved chip size area, power delay, power consumption and complexity etc.

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