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Design of Han Carlson Adder for Implementation of CSLA

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Abstract -*For different VLSI applications, such as image processing, video processing, Digital Signal Processor and microprocessors use carry select adder (CSLA) for various arithmetic functions. From the structure of regular SQRT CSLA, still there is possibility to get better design in which optimization of area, delay is to be major concentrations along with power requirement. Existing solutions used in SQRT CSLA is replacement of second level ripple carry adder (RCA) by binary excess converter (BEC). Though increases the performance, there is very less percentage of improvement in reduction of area required and also the existing adder with RCA technique at its first level of CSLA is not suitable for area efficient applications. Hence this paper proposes CSLA using Han Carlson design in place of first level RCA. In future, it can be observed from the results that the area and delay will reduce at comparable percentages with respect to RCA and BEC techniques, when HCA will use at the first level 32-bit SQRT CSLA. This proposed logic is designed using VHDL technology in the XILINX design suit.*

Key Words: **Han Carlson adder (HCA),carry select adder (CSLA), Regular SQRT CSLA, Ripple carry adder(RCA), Binary excess converter(BEC),etc.**

I.INTRODUCTION

Design of VLSI circuit with less area and high speed has become a main concern for digital designers. Designing area efficient VLSI systems has emerged as highly in demand because of the fast growing technology in mobile communications and computation. The design of mobile phone now becoming more and more slim and thinner. There is a limited amount of power availability in the mobile systems as the size of battery also reduced. That's why designers are facing more constraints such as high speed, high throughput and small silicon area. So building area efficient, high performance adder cells are of great interest. To reduce area requirements of the computational circuits, the size of transistors are reduced into the deep submicron area and commonly handled by process engineering. There are different types of Adder designs have been proposed and implemented to reduce the power consumption. Logic minimization results in better system throughput as well as area efficient designs. To achieve more speed CSLA is replaced by SQRT CSLA. The CSLA is used for computational systems to alleviate the problem of carry propagation delay by individually generating multiple carries and then select a carry to find out the sum. However, the CSLA is not area efficient as there are multiple pairs of RCA's to generate partial sum and also carry input Cin=0 and Cin=1, the final sum and carry are selected with the help of multiplexers. Section II of this paper reviews existing logic and section III explains about logic level modification in which replacement of first level RCA with HCA. Section IV represents results and comparisons. Finally the work is concluded in section V.

II. EXISTING LOGIC

In general the whole SQRT CSLA is divided into separate blocks. The size of block and the number of blocks rely on the size of SQRT CSLA corresponding to the SQRT technique. In this after second block, each block contains three different levels, first level is RCA with input carry zero, next level is ripple carry adder with input carry one at its carry in input and at the last level there is multiplexer which is to select either of the ripple carry adders output corresponding to the previous block carry out.

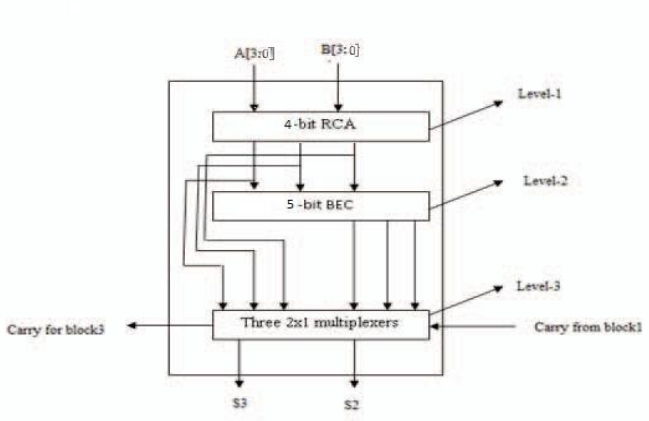

Fig. 1. Second block of SQRT CSLA with BEC instead of RCA in second level RCA

The drawbacks in SQRT CSLA are large area needed as it uses both levels of RCAs. For achieving increased area efficiency Binary to Excess-I Converter (BEC) is used in the place of RCA with carry input Cin=1 in the regular CSLA. For replacing n bit RCA an n+1 bit BEC is required.

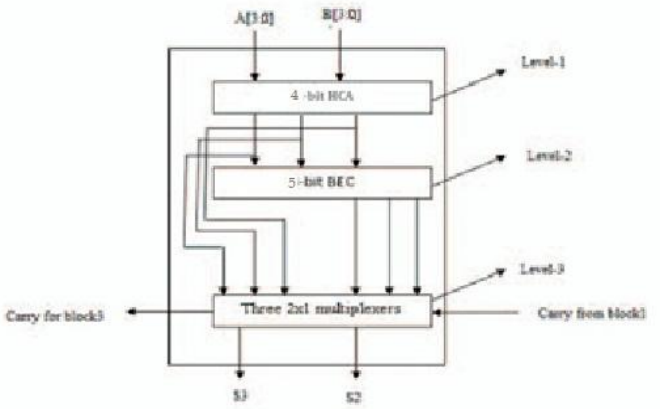

Fig. 2. Second block of SQRT CSLA with HCA in first level RCA

Second block of 4-bit SQRT CSLA with BEC logic at its second level is shown in fig.1. One input to the third level multiplexers is from output of first level RCA and second input is from BEC output. This delivers the two different partial results in parallel and the multiplexer is used to select one of two, the BEC output or the direct inputs corresponding to the control signal Cin.

III. PROPOSED LOGIC IMPLEMENTATION

Though BEC technique with RCA in second level of CSLA reduces area and power but not up to considerable amount and also the design is incompatible for sub threshold level modifications.

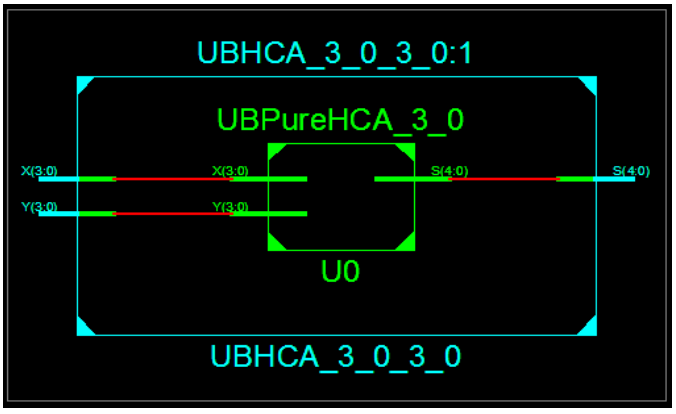

Fig 3.Verilog Implementation of 4 bit Han Carlson Adder

A. Han Carlson Adder for 4-bit

Han-Carlson prefix tree is same as that of Kogge-Stone's structure as it has a maximum fan out = 0 or fan-out of 2.Han-Carlson prefix tree is different between these two is that it uses much less cells and wire tracks compare to that of Kogge-Stone. In the expense of one extra logic level. Han-Carlson prefix tree is nothing but the sparse version of Kogge-Stone prefix tree. And in fact, the fan-out at all logic levels is the same.

Han-Carlson prefix tree can be easily built by modifying the pseudo-code for Kogge-stone's structure. The main difference is in each logic level, Han-Carlson prefix tree puts cells every other bit and the last one logic level accounts for the missing carries.

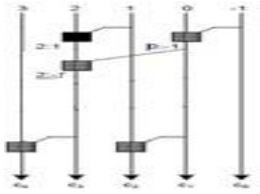

Fig 4.4-bit Han Carlson Prefix tree

Figure 4 shows a 4-bit Han-Carlson prefix tree, ignoring the buffers. In the fig. the critical path is shown by thick solid line. A good trade-off in between fan-out, number of black cells and number of logic levels is given by Han-Carlson.

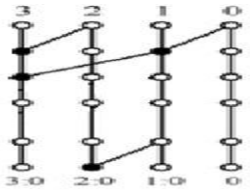

Fig 5. 4-bit Han Carlson Adder (Graph representation)

In Fig 5, The Han-Carlson adder uses only one Brent-Kung level at the beginning of the graph and at the end of the graph, and the number of levels in this is 1+ $log2(n)$.In this fig. black dots for the prefix operator, while white dots represent simple placeholders. The Han-Carlson adder consists of a good trade-off between fan-out, number of black cells and number of logic levels. Due to this, Han-Carlson adder can achieve similar speed performance as that of Kogge-Stone adder, at lower power consumption with area. Therefore it is possible to implement such a speculative Han Carlson adder

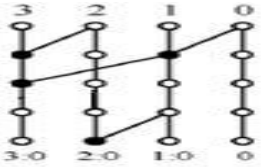

Fig 6 For 4-bit Han-Carlson prefix-processing stage

Fig 6 represents the Han-Carlson adder with two Brent-Kung rows at the beginning and at the end of the graph are as it is, though the last Kogge-Stone row is removed. Hence in general, one has $l=n/2^r$ where r is the number of removed levels; the number of levels of this Han-Carlson stage reduces from 1+ $log_2(n)$ to 1+ $log_2(l)$, assuming with l that is a power of 2.

In general, the computed generate and propagate signals for the speculative Han-Carlson architecture are:

- $(g,p)_{i:0}$ for: i < l
- $(g,p)_{i:i-l}$ for: i > l, i even
- $(g,p)_{i:i-l+1}$ for: i > l, i odd

B. SIMULATION AND RESULT

The Ideal N-bit tree adder includes:

- K= log N logic levels
- Fan-out of 2
- There is only than one wiring track between levels

There is requirement of large numbers of parallel wiring for wide bit in Han-Carlson adder. Hence packing the wires close to each other will increase the coupling capacitance on each wire. Han-Carlson become attractive one when interconnect is considered as it needs only half the number of columns. The Individual specifications are same as *Kogge-Stone* has minimum logic levels but lack to P and G. When it comes to logic levels *Han-Carlson* has more logic levels but least cells. *S. Knowles* having more cells, wires and some fan-out. The *Sklansky* having less logic levels and highest fan-out. Simulation and synthesis of this is done using Xilinx design suite 13.1.The abbreviations that are present in the following discussions are: HCA for the Han-Carlson adder and RCA for the ripple carry adder. Table.1 with the synthesis results of different adders, fig.7 with Test bench for HCA 4-bit and Table. 2 show the device utilization summaries.

Table 1 Comparison table on RCA and HCA

PARAMETER	RIPPLE CARRY ADDER	HAN CARLSON ADDER
NUMBER OF SLICES	2%	1%
NUMBER OF INPUT LUTs	2%	1%
NUMBER OF I/Os	10%	5%
DELAY ESTIMATION	16.689ns	7.898ns

Test Bench Waveform

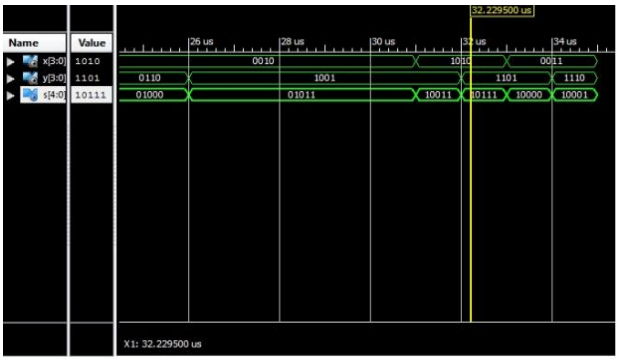

Fig 7. Test bench waveform of HCA

V CONCLUSION

The results presented significantly produced the efficiency of the proposed methodology. The performance evaluation of the simulated model would be good starting point of further research.

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