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EFFICIENT IMPLEMENTATION OF CASCADED IIR FILTER DESIGN AND A PARTITION MULTIPLIER

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Abstract -*This paper proposes a beneficial VLSI design for cascaded arrangement of a higher order IIR filter, which can be used in DSP applications like equalizer, loud speakers etc. The proposed configurable 6th order IIR design is arranged with three biquad filters. The same is utilized to perform one sixth order or three second order or one fourth order and one second order calculations in parallel.A multiplier is one of the key equipment pieces in most advanced and superior frameworks, for example, IIR channels, advanced signal processors and microchips and so on. With advances in innovation, numerous analysts have attempted and are attempting to plan multipliers which offer both of the accompanying rapid, low power utilization, normality of design and henceforth less area or indeed, even mix of them in multiplier.So in this paper we show another idea for fast multiplication of two numbers that avoids the overhead of long carry chains. Segment adders and multipliers can be a traded off and can be adopted based on the application demand.*

Key Words:IIR filters, Configurable design, Multipliers.

1.INTRODUCTION

Digital filters are necessary parts of numerous advanced signal processing frameworks, including control systems, systems for sound and video processing etc. Digital filters [2] are used to remove undesirable content of the digital signal. The infinite impulse response filter can be represented using the equation (1). The coefficients are given by ak and bk and M and N define the order of the filter. In this work we take M and N as equal (M=N=6)

$$y[n] = \sum_{k=1}^{N} a_k y[n-k] + \sum_{k=0}^{M} b_k x[n-k] \quad (1)$$

As we understand from the equation the operation of filter involves repetitivemultiplications and additions so we introduce an effective multiplier thatavoids long chains of carry. Parallel multiplication algorithms have been presented in [4],[5].The proposed multiplieris better than the present multipliers while achieving better performance only with an acceptable increase in the area. In this new assembly for multiplier inputs are parted into segments. Products are computed with no carries between partitioned segments of numbers. Component adders and multipliers to be used can weighedaccording to the application.The Dadda Tree multiplier is thought to be one of the speediest multiplier usages. Wallace Tree multiplier is like Dadda yet involve bigger area relatively. The speed offered by Dadda and Wallace multipliers comes at the expense of extra area. The proposed multiplier consequently offers a tradeoff amongst area and speed.

2. ThePROPOSED IIR FILTER

The proposal of biquad filter used in the arrangement isshown in the figure (1). Here b0, b1, b2, a1 and a2 are filter coefficients. The input and output signal example qualities are spoken to as x(n) and y(n) separately.

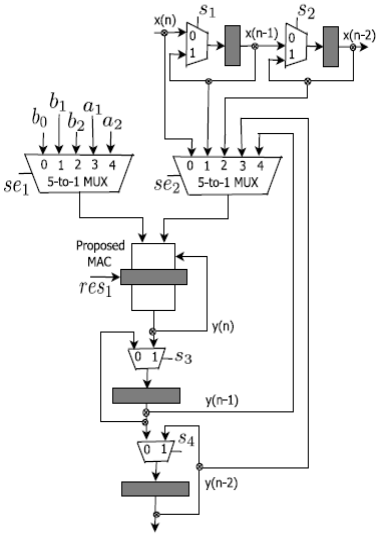

Fig. 1. Proposed IIR filter design

Here multiplexers assume the significant part, which choose the proper input/yield signal example values and coefficients for every clock cycle. The condition (2) demonstrates the second order IIR channel operation.

$$y(n) = a_1 y(n-1) + a_2 y(n-2) + b_0 x(n) + b_1 x(n-1) + b_2 x(n-2) \quad (2)$$

2.1 Proposed multiplexer based cascaded filter design

The proposed configurable IIR design outline is appeared in Fig. 2, where three biquad IIR channels (F1, F2 and F3) are bought together to perform three different modes of operations.

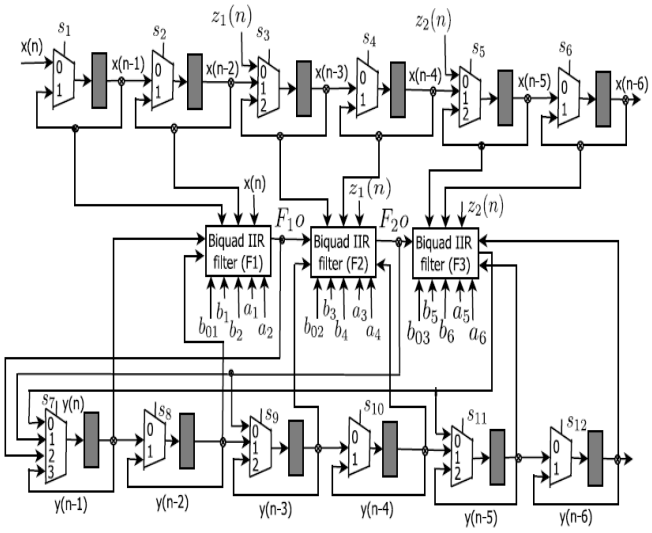

Fig. 2. Cascaded structure of 6th order filter.

The proper select lines of the multiplexers are utilized to perform one specific mode for IIR design appeared in table 1.

Table -1: Different modes of operation

IIR Filter Operation	S3	S5
F1,F2,F3 are used for 6th order	1 or 2	1 or 2
F1 and F2 are used for 4th order and F3 used for 2nd order	1 or 2	0 or 2
F1,F2,F3 are used for 2nd order	0 or 2	0 or 2

Proposed sixth order IIR filter can be given as y(n) = a1y(n-1)+a2y(n-2) +a3y(n-3)+ a4y(n- 4)+a5y(n-5)+a6y(n-6)+b0x(n)+b1x(n-1)+b2x(n-2)+b3x(n3)+b4x(n-4)+b5x(n-5)+b6x(n-6). Here the terms a1y(n-1), a2y(n-2), b0x(n), b1x (n-1) and b2x(n-2) can be found by biquad F1.The terms a3y(n-3), a4y(n-4), b3x(n-3) and b4x(n-4) can be found by biquad F2. Essentially the terms a5y (n-5), a6y (n-6), b5x(n-5) and b6x(n-6) can be found by biquad F3.

3. PROPOSED PARTITION MULTIPLIER

The fig. 3. presents the partition multiplier. Here first step involves the portioning of the larger number into smaller segments. The partitions are interlaced and are multiplied using the component multipliers. Then the obtained products are concatenated and shifted and are aggregated to get the final product of the taken two large numbers. Here in this example we consider two 32 bit numbers.

Here the quality r, speaks to the quantity of bits that are contained by the partitioned number. The quality s, speaks to how frequently the bigger number is being apportioned. The proposed multiplier is effective when contrasted with the other existing multipliers. The power utilization of the allotment multiplier 0.022Watts contrasted with the Wallace Tree Multiplier that gives 0.087 Watts of utilization and Booth Multiplier that devours the power of 0.97Watts.

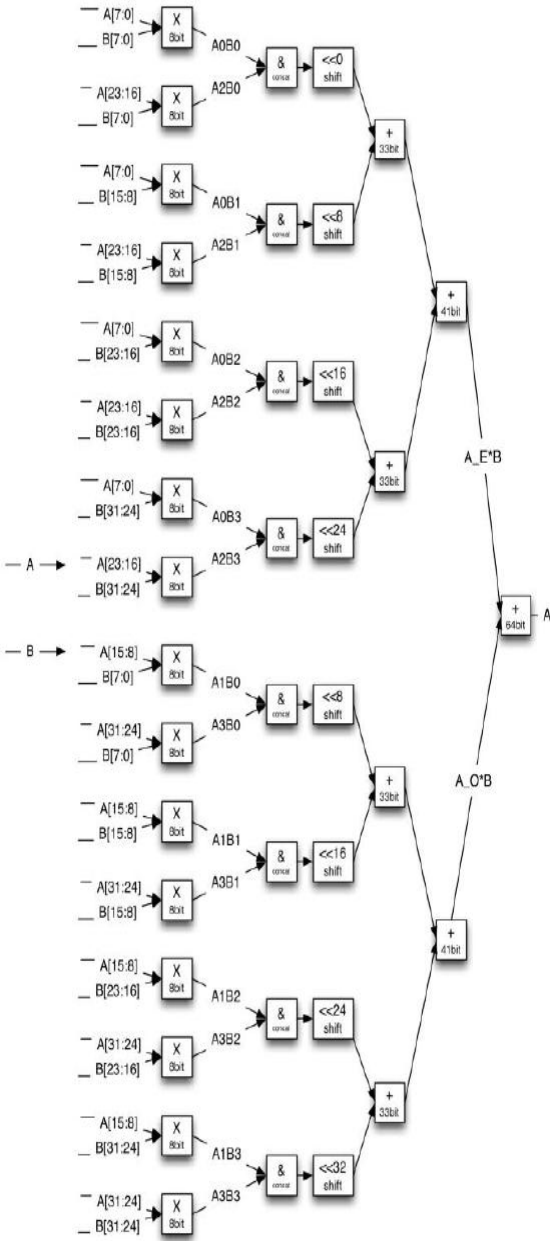

Fig.3.Figuredepictingtheidea of partition multiplier

4. IMPLEMENTATION AND RESULTS

All the current and proposed plans are displayed in Verilog HDL.These Verilog HDL models are simulated and checked utilizing Xilinx ISE simulator. The synthesis of all these designs is done with Cadence RTL Compiler. Programming modules created are for Field programmable gate array (FPGA). The modules delivered the precise outputs when they were cross verified with the design flow. We mention examinations. The Partition multiplier in gives a tradeoff between fast and low chip designs. The area in which it is a decent decision turns out to be more proclaimed as the quantity of bits increment and presents interesting tradeoff for 32 and 64 bit cases. By utilizing diverse segment adders and multipliers, furthermore, through recursive usage at higher quantities of bits, the Partition multiplier can be streamlined for a given application as far as the tradeoff amongst area and speed.

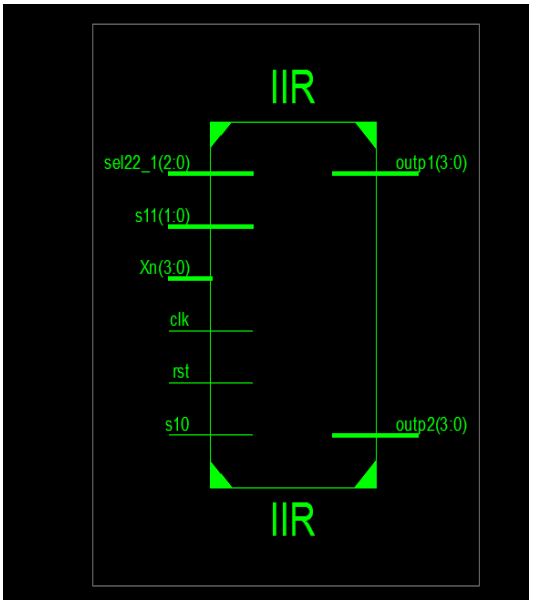

Fig. 4. Module for IIR filter design

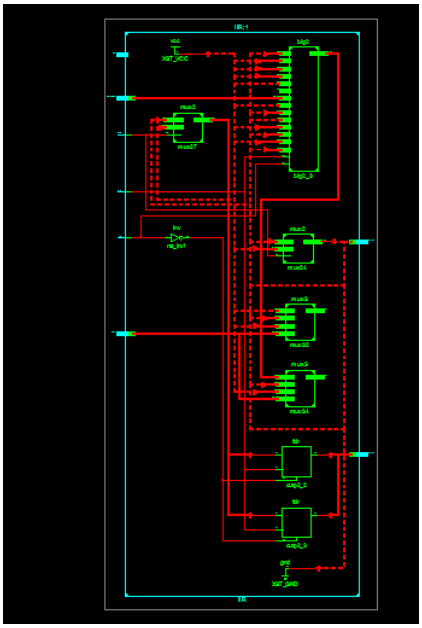

Fig.5. Synthesized Circuit of proposed IIR Filter design.

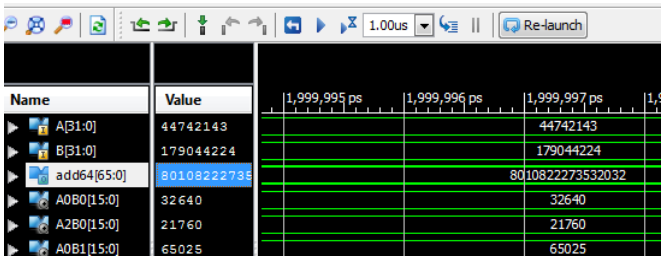

Fig.6. Partition Multiplier simulation window

5. CONCLUSIONS

This paper proposes an efficient VLSI configurable IIR design. The proposed configuration depends on multiplexers and based on the select lines of the multiplexers the three biquadfilters can work to perform in three unique modes. Circuits intended to perform multiplication are broadly utilized as a part of advanced filters. Subsequently, we find that the Partition multiplier, which can enormously lessen the lengths of the long carry chains in multiplier. For outlining a tradeoff amongst speed and chip area is critical. The partition multiplier offers tradeoff between the slow but cheap array multipliers and the quick yet vast Dadda or Wallace Tree multipliers. The decision for component multipliers must be surrendered over to the application-particular cost capacity.The future work that can be completed will be the executing of the partition multiplier in the proposed filter configuration which will increase the proficiency of the filters.

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