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Design of the Fully Functional Trellis Encoder Decoder Using Verilog HDL

AbhinavRanjan[1], Praveen Kumar N[2], Hemanth Kumar K S[3]

[1]PG Scholar,Digital Electronics, VTU, VTU Extension Centre UTL technologies LTD, Bangalore
[2]PG Scholar,Digital Electronics, VTU, VTU Extension Centre UTL technologies LTD, Bangalore
[3]Assistant Professor, Digital Electronics, VTU Extension Centre UTL technologies LTD, Bangalore

Abstract-This paper presents the architecture of fully functional Trellis Encoder-Decoder to encode and consequently decode the encoded data using Trellis based algorithm. Traditional Convolution Encoder's modified structure termed as Trellis Encoder is described with constraint length K=3, and code rate r=1/2, simultaneously the algorithm used to decode them is also emphasized in one of the sub-section. The Trellis Encoder-Decoder is targeted for the Xilinx Spartan6 FPGA (Field-Programmable Gate Array) and is designed with Verilog HDL (Hardware Description Language). Simulation results and concerning schematic and device utilization summary report of the above mentioned design is obtained using Xilinx ISE (Integrated Synthesis Environment) design tool.

Keywords-Traditional Convolution Encoder, Trellis Encoder, Trellis Decoder, Constraint Length, Code Rate, Verilog HDL

1. INTRODUCTION

Convolution coding is a most admired and well accepted error-correcting coding method in digital communication system. A message is convolved using binary convolution method that is simply xor (exclusive-or) operation, and then this encoded information is transmitted into a noisy channel. This convolution operation encodes some redundant information into the transmitted signal, thereby improving the data capacity of the channel. But the shortcoming of traditional Convolutional Encoder is lack of randomness in the encoded data which makes it vulnerable to the channel noise [1]. Hence in order to make it robust to the channel noise the recursive procedure is introduced in the encoder section that is termed as Trellis Encoder. The trellis decoding algorithm tracks down the most likely state sequences the encoder went through in encoding the message by means of nodes processing and uses this information to determine the original message and to separate the redundant bits introduced. Instead of estimating a message based on each individual sample in the signal, the trellis encoding and decoding process packages and encodes a message as a sequence, providing a level of correlation between each sample in the signal. As the convolution codes are used widely for the channel encoding of data to achieve low-error-rate in latest wireless communication standards for example 3GPP, GSM and WLAN; the use of optimal decoding algorithm satisfies the requirement of these applications convincingly.

2. DESIGN ARCHITECTURE

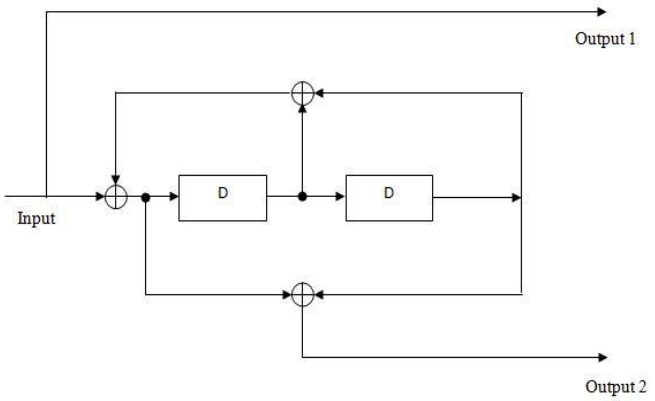

Fig.1 Trellis Encoder

The Traditional Convolutional Encoder is changed to a Trellis Encoder by feeding back the first output of the encoder to one of its input. Hence, the generator matrix of the encoder will change as following:

$$G= [1, g1/g2]$$

Here the number 1 indicates the systematic output whereas g1/g2 indicates the feed forward output. The method of getting the encoded output is slightly customized with compare to the traditional Convolutional Encoder. Here one of the output is directly feedback to the input, while other one is obtained with the modulo-2 addition and then repeating iterative procedure. At last both the outputs are obtained from the encoder by multiplexing the otutput1 (systematic data) and output 2(feedforward output) bit by bit. The resultant Trellis encoder of r=1/2 and constraint length K=3 is depicted above in Figure 1.

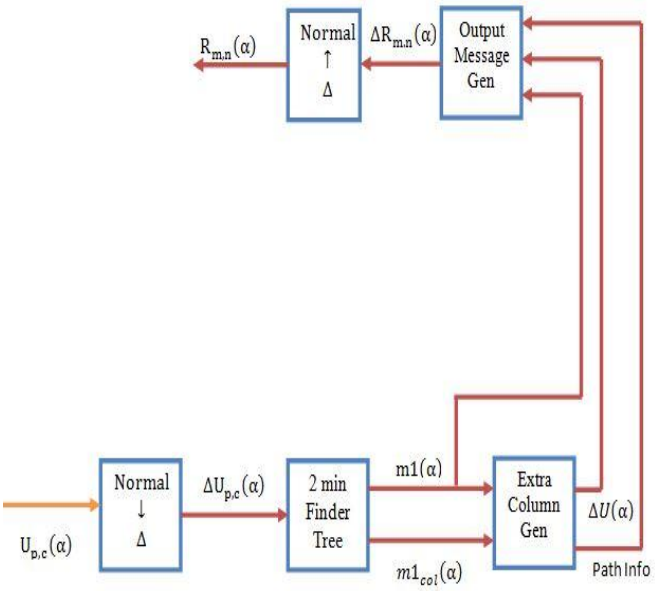

Fig 2.Trellis Decoder

The output of the encoder is received at the input of the decoder where the received message is termed as normal domain message this gets converted through permutation network by newly defined vector message domain called as delta message domain. In this delta message domain the messages are transformed with the field value which has the maximum reliability as the reference. The output of this block is given to the next stages comprising of 2 min finder tree and the extra column generator. The output of these stages are going to be generated as the output message in the delta domain, consequently by using the permutation network the delta domain message (most reliable) is converted back in to the normal domain and this is the resultant output of the decoder which is originally the input to the encoder.

3. RESULT

The simulation result in Figure 3 is obtained by the implementation of the fully functional Trellis Encoder and Decoder. The Figure 4 shows the detailed RTL schematic of the proposed design and the device utilization summary report generated by Xilinx ISE design tool is given in Table 1.

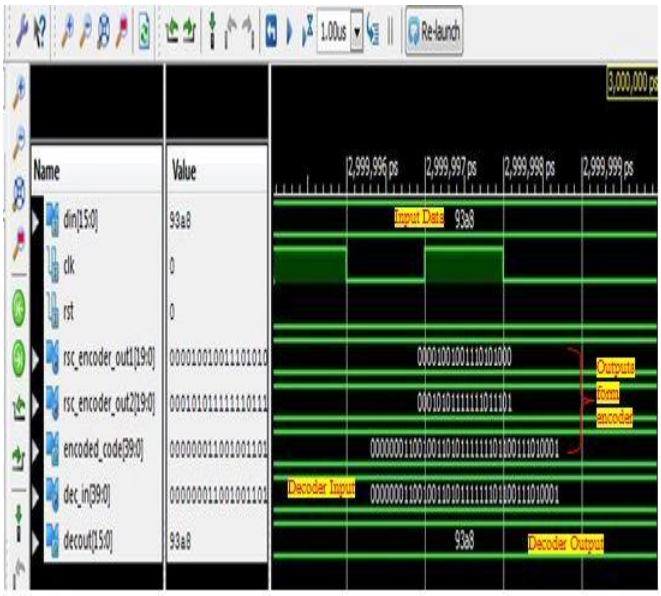

Fig.3 Simulation Result of the Trellis Encoder-Decoder

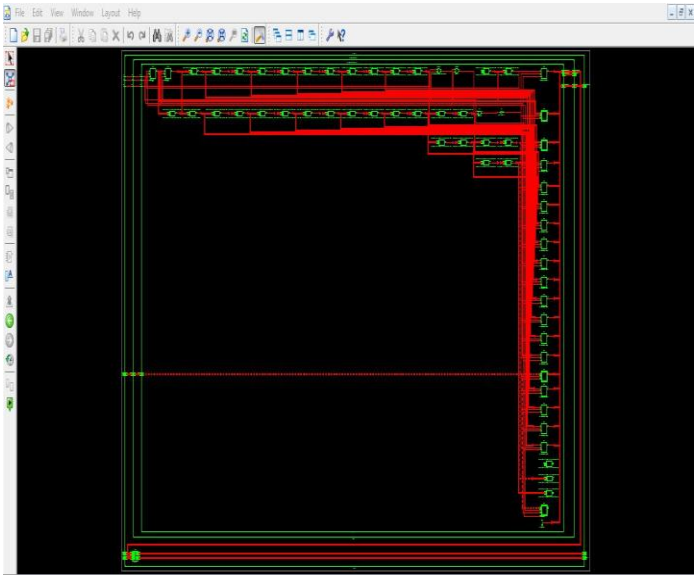

Fig. 4RTL Schematic of the Trellis Encoder-Decoder

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	20	54576	0%
Number of Slice LUTs	40	27288	0%
Number of fully used LUT-FF pairs	19	41	46%
Number of bonded IOBs	99	296	33%
Number of BUFG/BUFGCTRLs	1	16	6%

Table 1 Device Utilization Summary Report of theTrellis Encoder- Decoder

4. CONCLUSION

The fully functional Trellis Encoder Decoder using Verilog HDL is implemented and the simulation result with the associated schematic and device utilization summary report are presented in the paper. The utilization for Trellis Encoder and Decoder for slice registers and LUTs is less than 1% which comprises of total logic to be implemented hence making it an efficient architecture also.

REFERENCES

[1] Rajagopal.A, Karibasappa.K, Vasundra Patel K.S, "FPGA Implementation of a Modified Turbo Encoder", IJCA(0975-8887), vol.116, no.6,2015
[2] AlexandreGraelliAmat , Fredrik Brannstrom , Erik Agrell, "An Asymptotically Optimal TCM Encoder", IEEE trans. on communications vol.61 , issue.6,2013.
[3] GanesanThiagarajan, Chandra Murthy, "Trellis coded block codes and applications", NCC 2009, January 16-18, I IT Guwahati
[4] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near Shannon limit error correcting coding and decoding: Turbo-codes.1,"Communications, 1993.ICC93.Geneva.vol.2, pp. 1064–1070.
[5] D. J. MacKay and R. M. Neal, "Near Shannon Limit Performance of Low Density Parity Check Codes," Electronics Letters, vol. 32, pp.1645–1646, 1996.

[6] N. Wiberg, "Codes and Decoding on General Graphs," Ph.D. dissertation, Linkoping University, Sweden, 1996.
[7] D. MacKay,"Good Error Correcting codes based on very Sparse Matrices, "IEEE Trans. inform Theory, vol. vol.46, pp. 399–431, Mar 1999.
[8] R. G. Gallager, "Low-Density Parity-Check Codes," Cambridge, MA: MIT.Press, 1963.
[9] M. Luby, M. Mitzenmacher, M. A. Shokrollahi, and D. A. Spielman, "Analysis of low density codes and improved designs using irregular graphs," STOC, pp. 249–258, 1998.
[10] T. J. Richardson and R. L. Urbanke, "The Capacity of Low-Density Parity Check Codes Under Message-Passing Decoding," IEEE Trans. Inform. Theory, vol. 47, pp. 599–619, February 2001.