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DESIGN AND IMPLEMENTATION OF 3D 4x4 MESH TYPE BUFFERLESS NOC USING X-Y ROUTING ALGORITHM

SUSHMA N, NEETHU K N

MTech student, VLSI and Embedded Systems, Dept of ECE, Reva Institute of Technology and Management,Karnataka, India
Assistant Professor, VLSI and Embedded Systems, Dept of ECE, Reva Institute of Technology and Management,Karnataka, India

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Abstract - *A basic 3D NOC Router has problems of deadlock and hot spot. Also it requires buffers to store packet data. In this paper we present 3D 4 *4 NOC Router which uses routing algorithm called X-Y Routing algorithm which will avoid deadlock and hot spot by using priority encoders. The 3D NOC Router designed here is also buffer less since the data is transferred at a speed of 1clock per node and does not require buffers to store data. The 3D NOC router is designed using Verilog HDL, simulated by Modelsim and prototyped by using FPGA. The simulation results show that it also improves the area utilization.*

Key Words: **3D NOC, X-Y Routing,deadlock,hotspot**

1.INTRODUCTION

Network on Chip(NOC) is a subsystem on an integrated circuit which acts as a communication interface between nodes in a System on Chip(SOC).SOC is an integrated circuit that combines all components of electronic system into one chip. Performance of a NOC depends strongly on its underlying architecture and routing techniques. Here we are building 3D NOC by using 2D NOC's. 2D NOC's are placed vertically one above another instead of placing them next to each other, thereby forming a 3D NOC. Compared to 2D NOC, 3D NOC has minimum latency, lower power consumption, better performance and increased area utilization.

Due to constraints such as wire-length constraints and layout complications, the 2D NOCs have limited network structures that are possible. There are various types of 3D NOC topologies such as 3D Mesh, 3D Torus, 3D Stacking Mesh and so on.

We are using a 3D 4x4 Mesh type NOC which consists of nodes and routers. Each node also has a priority encoder

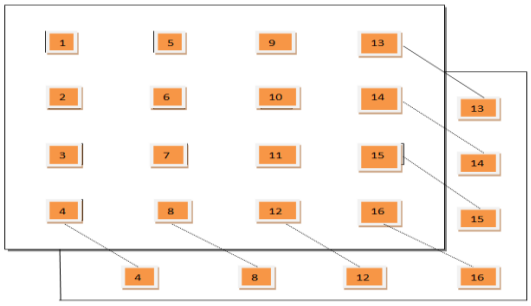

Fig-1: 3D 4x4 Mesh type NOC

Router is the most important component for transferring data from one node to another. It is the communication backbone of a NOC system. So it should be designed with maximum efficiency. Routers are used on a network for directing the traffic from the source to the destination. It coordinates the data flow which is very crucial in communication networks.

Routers are intelligent devices that receive incoming data packets, inspect their destination and figure out the best path for the data to move from source to destination. Router must be well designed to achieve high performance.

The *priority encoders* output corresponds to the currently active input which has the highest priority. So when an input with a higher priority is present, all other inputs with a lower priority will be ignored.

1.1 RELATED WORK

Different types of routing algorithms have been mentioned by other papers

Paper [1] shows a router which uses a Elevator-first routing algorithm which transmits packets to the destination node in an irregular topological structure. But this algorithm suffers from deadlock.

Paper [2] shows a router which uses look ahead XYZ routing algorithm, which reduces the power consumption but it occupies significant area since it uses input buffer. So it is not buffer less.

Paper [3] addressed the thermal power problem in 3D NOC's which is one of the most important issues in 3D NOC's. The routing algorithms which are used takes too many

vertical hops for the packet to reach its destination, even when source and destination are located on the same layer.

Paper[4] uses a routing algorithm called Randomized Partially Minimal (RPM) which balances the traffic along the network. It will send packet to a random layer first, then along the X-Y dimensions and finally to their destination along the z-dimension.

Paper [5] shows a hierarchical router for 3D NOC. Compared to other routers this type of router has 2 decoupled modules one for intra layer and other for inter layer. It has 30% more throughput and 30% more latency than 3D Mesh NOC's.

Paper[6] aims to reduce the number of vertical links in 3D Mesh type NOC's but do not give the proper details of the routing algorithm.

Paper [7] demonstrates a 3D stacked router. They have proposed a router called MIRA where it is stacked into multiple layers to reduce area and power consumption. They show the results of 3 types of 3D routers(a)3D baseline router(3DS)(b)3D multilayered router(3DM)(c)3D multilayered router with express paths(3DM-E).

Paper [8] It demonstrates a router following a Adaptive Z routing algorithm which is a bus failure tolerant algorithm. It shows that performance is much better than symmetric NOC, 3D Mesh and Hybrid NOC bus based 3D-Mesh.

Paper [9] In this paper they have proposed a deadlock free router using a Negative-First algorithm. It uses a dynamic arbiter and a priority scheduler module. But the fault tolerant mechanism needs to be developed.

Paper [10] In this paper a combined mapping and routing algorithm based on Answer set programming (ASP) has been proposed. It provides vast routing options.

Paper [11] In this paper a routing algorithm which is based on geometrical arrangement for 3D NOC is proposed. In this algorithm, the geometrical space is partitioned into quadrants and the nearest wrap around edge is selected to reach the destination.

Paper [12] In this paper a partially connected 3D crossbar structure called 3D Dimensionally-Decomposed (DimDe) router has been proposed. Virtual channels are utilized to avoid congestion and separation of router architecture into 3 modules has been done. The router architecture is very complex but it improves latency.

1.2 X-Y ROUTING ALGORITHM

The X-Y Routing algorithm is as follows.

1. Destination z is compared with the current z, if it is same it belongs to the same plane
2. If not, if destination z > current z, then move up else move down.
3. Now check for x, if destination x is same as current x then it belongs to same column.
4. Else, check if destination x > current x, if yes then move east else move west.
5. Now check for y, if destination y is same as current y then it belongs to same row.
6. Else check if destination y > current y, if yes move south else move north

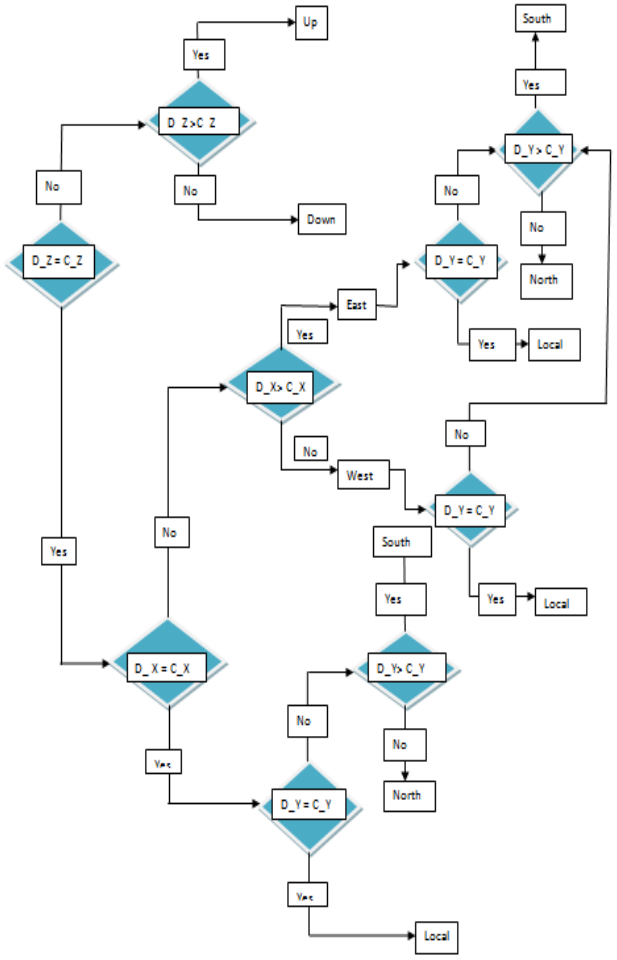

Fig-2: X-Y Routing Algorithm

2. IMPLEMENTATION OF 3D 4*4 MESH TYPE NOC

Basically 3D 4x4 Mesh type NOC is constructed by placing two 2D 4x4 NOC placing one above another. Each node in 3D NOC has a router and a priority encoder

A.ROUTER DESIGN

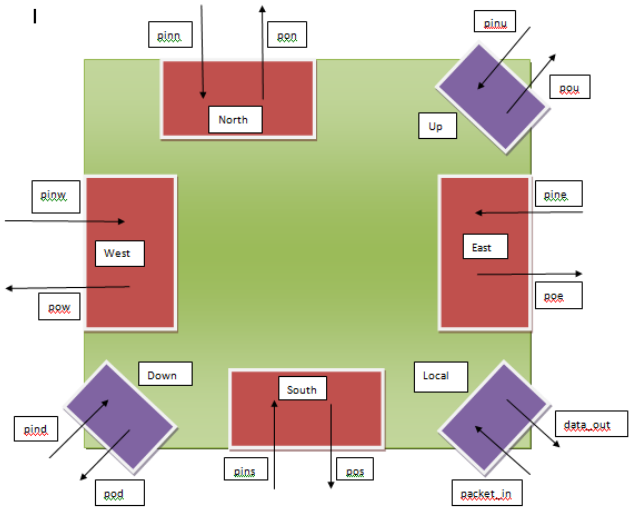

Fig-3: Router Design

The router design for 3D NOC has 7 input-ports and 7 output-ports whereas 2D NOC has 5 input-ports and 5 output-ports which are north, south, east, west and local. The 3D NOC has 2 extra input and output ports which are up and down to the router. Each port has input and output pins.

B.PRIORITY ENCODER

A Priority encoder is an encoder circuit that includes the priority function. A encoder is a digital circuit that performs the inverse operation of a decoder. In encoder the output lines generate the binary code corresponding to the input value. In priority encoder, if two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence. Each node has a priority encoder, due to this there is no deadlock.

3. SIMULATION RESULTS

The 3D NOC router is designed using Verilog HDL, simulated by Modelsim and prototyped by using FPGA.To verify the X-Y Routing algorithm, we can run the simulation results. Suppose packet_in is given to node 1 in the top plane, we will see how it is transmitted to node 16 in the bottom plane.

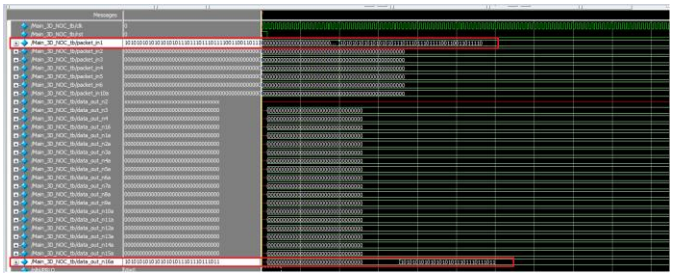

Fig-4:Simulation showing data transmission from input node(n1) on top plane to output node(n16)on bottom plane

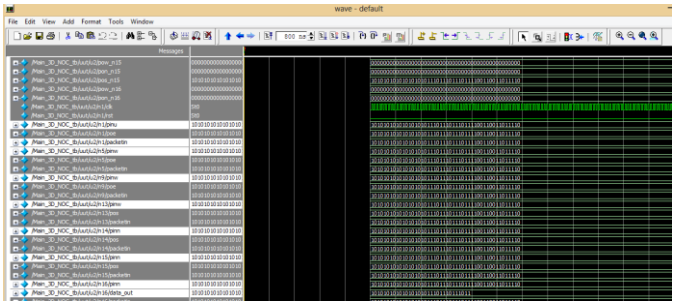

Fig-5: Simulation showing data transmission from input node(n1)on top plane to output node(n16)on bottom plane depicting data path through input pins of intermediate nodes(n1,n5,n9,n13,n14,n15,n16)

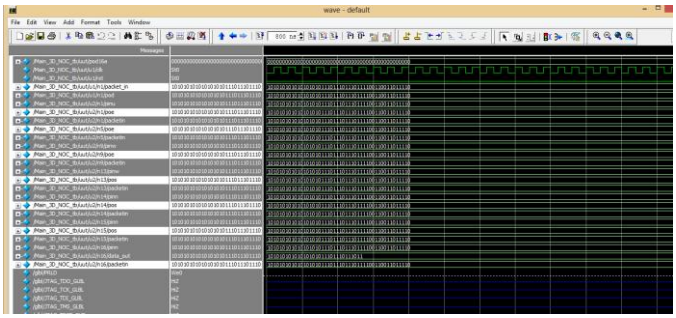

Fig-6:Simulation showing data transmission from input node(n1)on top plane to output node(n16)on bottom plane depicting data path through output pins of intermediate nodes(n1,n5,n9,n13,n14,n15,n16)

The design and timing summary for 2D 4x4 NOC is shown below. The maximum operating frequency for 2D 4x4 NOC is 382 Mhz

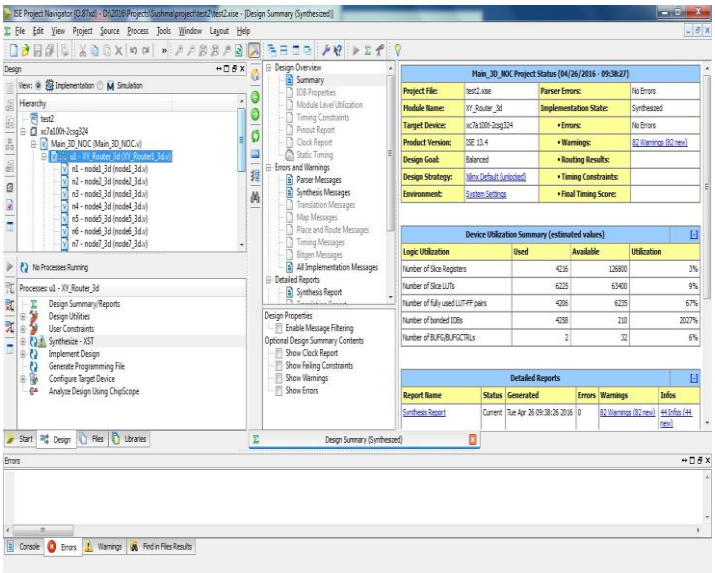

Fig-7: Design summary for 2D 4x4 NOC

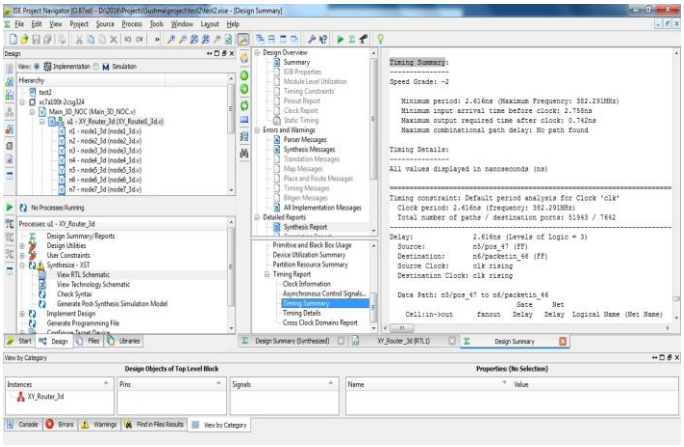

Fig-8: Timing summary for 2D 4x4 NOC

The design and timing summary for 3D 4x4 NOC is shown below. The maximum operating frequency for 3D 4x4 NOC is 378 Mhz

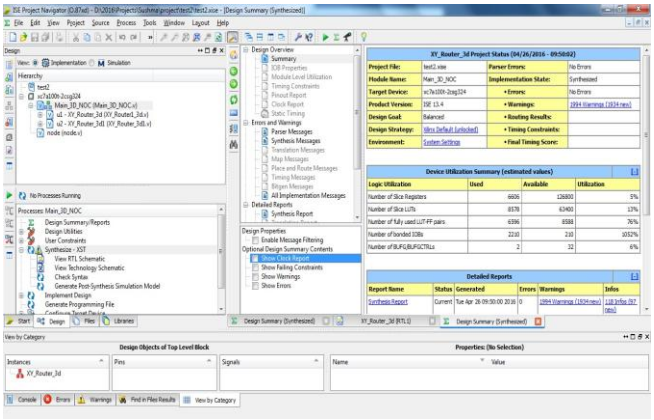

Fig-9: Design summary for 3D 4x4 NOC

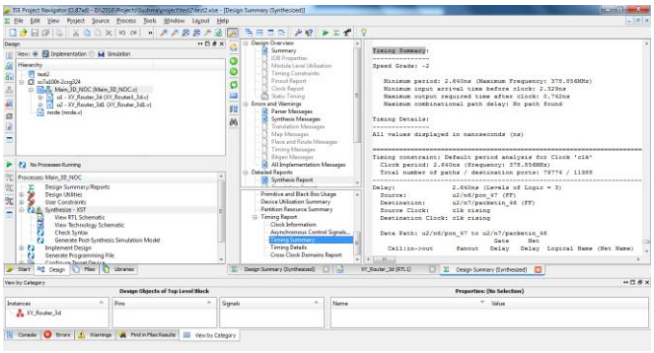

Fig-10: Timing summary for 3D 4x4 NOC

The internal architecture for 2D 4x4 NOC and 3D 4x4 NOC is shown below

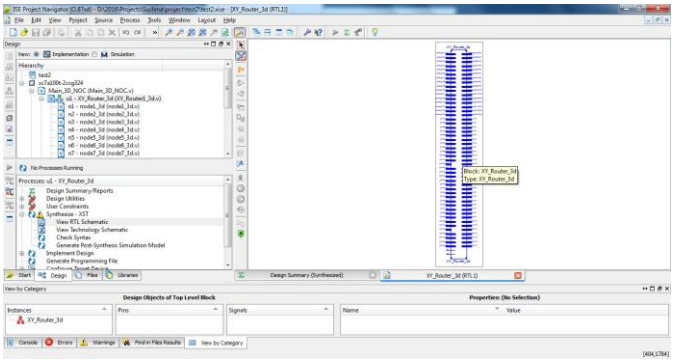

Fig -11: Internal Architecture for 2D 4x4 NOC

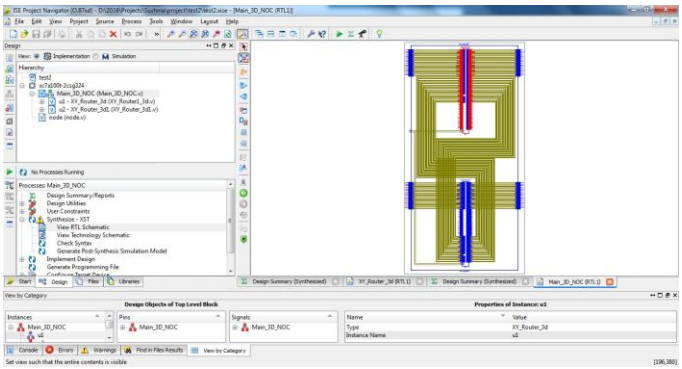

Fig-12: Internal Architecture for 3D 4x4 NOC

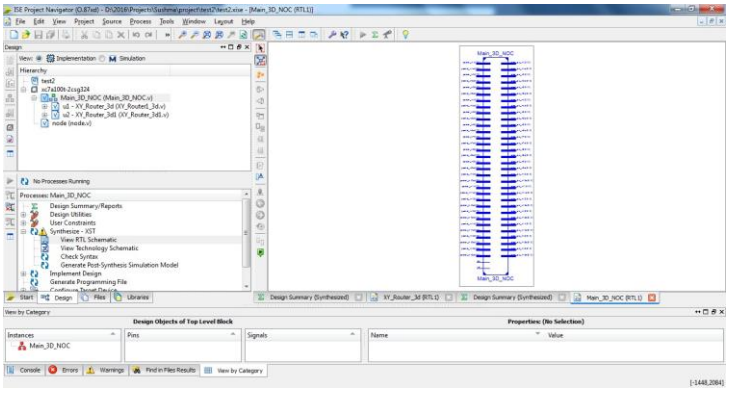

Fig-13: Top level RTL for 3D 4x4 NOC

4. CONCLUSION AND FUTURE WORK

The 3D NOC router is designed using Verilog HDL, simulated by Modelsim and prototyped by using FPGA. 3D 4x4 Mesh type NOC is constructed by placing two 2D 4x4 NOC placing one above another. Router uses routing algorithm called X-Y Routing algorithm which will avoid deadlock and hot spot by using priority encoders .Router designed is buffer less since the data is transferred at a speed of 1clock per node and does not require buffers to store data. This is an improvement over other NOCs since it saves a lot of memory and improves performance. The simulation results show that it also improves the area utilization. The future work

involves extending the number of nodes to 5x5 ,6x6 and so on and also increasing the layers vertically above one another.

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