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VLSI IMPLEMENTATION OF CMOS ANALOG MULTIPLIER

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Abstract - *A new CMOS voltage-mode four-quadrant analog multiplier is proposed and analysed. It is a VLSI based low voltage low power CMOS four quadrant analog multiplier. MOSFETs in the circuit used are in the strongly inversion saturated mode. The circuit uses simple 2-input "combiner" and "subtractor" cells connected in a novel topology. The proposed circuit will be useful in RF signal processing, AM modulation, half wave rectifier, etc. A low voltage high performance CMOS four quadrant analog multiplier is designed and fabricated by using 0.35 micron technology. The measured 3db bandwidth is 130MHz simple structure, low – voltage, low power, and high performance makes the proposed multiplier quite feasible in many applications.*

Key Words: Analog Multiplier1, Voltage Mode2, Four Quadrant, Low Voltage3, Low Power4

1. INTRODUCTION

Analog multiplier is an important building block in communication system like analog signal processing system; for example frequency mixer, variable gain amplifier, adaptive filters phase-locked loop, amplitude modulator, frequency doublers, rectifier, and demodulators etc. It is necessary to design an analog multiplier circuit which is suitable for low power low voltage and high speed application with better linearity.

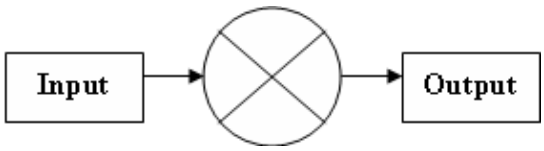


Figure 1: Basic Multiplier symbol

Depending on the input/output, analog multipliers can be classified as, Voltage Mode Multipliers [1] and Current Mode Multipliers [2].

Voltage mode multipliers:

$V_{i/p} = V_x$ and V_y;

$I_{i/p} = I_x$ and I_y;

$V_{o/p}=K*V_x*V_y$; $V_{o/p} =K*I_x*I_y$.

Current mode multipliers:

$I_{i/p} = I_x$ and I_y;

$V_{i/p} = V_x$ and V_y;

$I_{o/p}=K*V_x*V_y$; $I_{o/p} =K*I_x*I_y$.

In this paper, a low voltage, low power, high linearity and high speed multiplier circuit which operates in the voltage mode using parallel connected MOS devices at the input side and diode connected MOS devices as a load a the output side.

And also depending on the circuit configuration it can be classified as

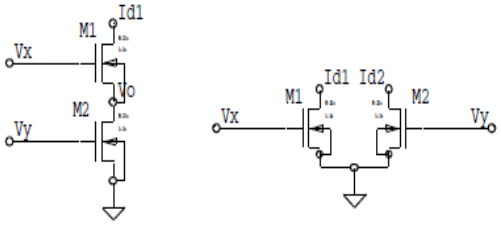
- Single balanced (2-quadrant), and
- Double balanced (4-quadrant) multipliers.

Quadrant based classification of multipliers is as follows:

- One-quadrant multipliers: Inputs are of the same phase
- Two quadrant multipliers: Opposite voltage can be added to either of the input
- Four quadrant multipliers: Opposite voltage can be added to both the inputs.

1.1 Performance Matrices of Analog Multiplier [3]

Linearity, supply voltage, power dissipation and noise are the main metrics of performance. We should try to design some specific structure or topologies for analog multiplier that have low power dissipation while at the same time ensuring good linearity , low supply voltage and low noise are kept at acceptable levels.



Cascade structure Parallel structure

Figure 2: Basic circuit configuration

Drain current during saturation and linear region is represented as below,

$I_d = 1/2\ K'(V_{gs} - V_{th})^2\ (1+\lambda V_{ds})$
$I_d = K'[(V_{gs} - V_{th})V_{ds} - 1/2V_{ds}^2]$

Where $K' = \mu_o C_{ox}\ W/L$ and V_{th} are the trans-conductance parameter and threshold voltage of the device respectively and λ represents the channel-length modulation effect for long channel devices. By biasing the transistors to operate in the triode region, we can reduce the drain current while keeping a relative large input range.

1.2 Four-Quadrant Multipliers using Series Connected Transistors

A voltage mode four quadrant analog multiplier based on a basic NMOS differential amplifier[1] that can produce the output signal in voltage form can be constructed using four one-quadrant multipliers or by using two two-quadrant multipliers as shown in Figure 3.

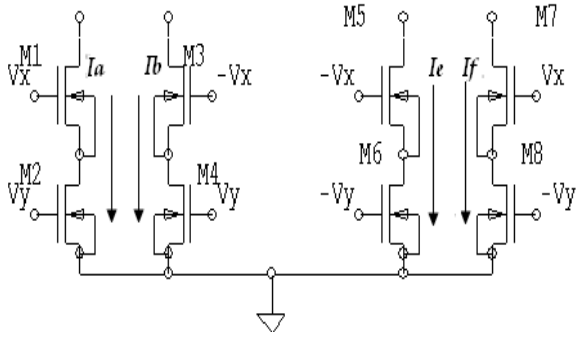


Figure 3: Four-Quadrant Multiplier

2. Basic Principle of Operation

Figure 2 shows how transistors can be used to implement multipliers. In order to reduce the number of devices parallel structure is useful compared to cascaded structure. The basic block diagram of four quadrant voltage mode multiplier is shown in Fig.3. The purpose of implementing this structure is to reduce the number of devices with minimum size.

The multiplier structure recommended in [4] uses NMOS as a load with constant V_{bias} voltage to operate the loads in saturation region and all the input transistors in the linear region. The only disadvantage of this structure is even though the number of devices is six; it requires additional devices for generating the bias voltage, which makes device count more than six. Using the same concept new structure is proposed to eliminate the V_{bias} sources. Hence the number of devices required for proper operation is only six. Here instead of using NMOS at the load side PMOS are used because of its negative threshold voltage.

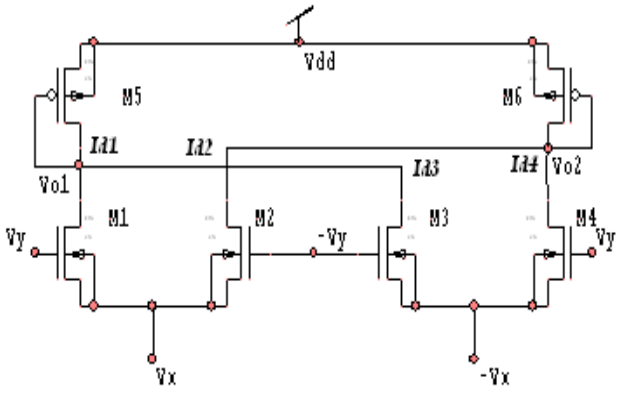


Figure 4: Proposed multiplier structure

2.1 Basic Multiplier

Figure4. Shown below is our proposed multiplier. It utilizes the low voltage of 1.2V and low power of 170 μw. As explained earlier it is designed using basic combiner and subtractor cells for operating in four quadrants. As seen from figure below there are two combiner and four subtractor cells are used. Hence it is a CMOS circuit which is designed using both PMOS & NMOS as its circuit elements. In this circuit we are replacing the four input combiners by the new proposed subtractor circuit's results in a new compact four-quadrant analog multiplier.

Differential input voltages, defined by $V_{id1} = V_1 - V_2$ and $Vid2 = V3 - V4$, are applied to input terminals of the four subtractor cells, the outputs of which are connected to input terminals of the two combiner.

The final output of multiplier is defined by $V_{out}=V_{01} - V_{02}$ taken from the outputs of combiner cells as shown in figure. In order to bias the circuit to operate in the saturation region, the minimum supply voltage requirement is

$V_{DD} = 2V_{effp} - |V_{tp}|$

Where, V_{effp} is the effective (or saturation) voltage of the *p*-channel devices.

Applying (3.2) and (3.5) to the circuit in Fig. 4.4, we can find the output voltages of the multiplier as follows-

$$V_{o2}=V_{DD}-k_nR\,[(V_3 -V_1 + V_{DD} -V_{tn})^2 + (V_4 - V_2 + V_{DD} - V_{tn})^2]$$

$$V_{o2}=V_{DD}-k_nR[(V_{31}+V_{DD} - V_{tn})^2+(V_{42}+V_{DD}-V_{tn})^2]$$

Put

$$V_{os} = V_{DD} - V_{tn}$$

Where, Vos is an undesired offset term which can be eliminated by fully differential operation.

$$V_{o2}=V_{DD} - k_nR[(V_{31}+V_{os})^2+(V_{42}+V_{os})^2]$$

$$V_{02}=V_{DD}-k_nR\,[\,V_{31}^2 + V_{42}^2 + 2V_{0S}(V_{31} + V_{42}) + 2V_{OS}^2] \quad .....(3.6)$$

Similarly, we can solve for V_{01} and it is given by-

$$V_{01}=V_{DD}-k_nR[\,V_{41}^2 + V_{32}^2 + 2V_{0S}(V_{41} + V_{32}) + 2V_{OS}^2] \quad .....(3.7)$$

The differential output voltage of the multiplier may be found by subtracting (3.6) from (3.7), yielding

$V_{out} = V_{o1} - V_{02}$

After solving we get

$$V_{out}=k_nR(V_{31}^2+V_{42}^2-V_{41}^2-V_{32}^2)$$

Now putting values of $V_{31} = V_3 - V_1$ and so on for all others, we get

$$V_{out}= -2\,k_nR(V_1 \times V_3 + V_2 \times V_4 - V_1 \times V_4 - V_2 \times V_3)$$

i.e. $V_{out}= -2\,k_nR[(V_1 - V_2)(V_3 - V_4)]$

But we have defined that $V_1 - V_2 = V_{id1}$ & $V_3 - V_4 = V_{id2}$ are the differential input voltages.

Hence we get final output of multiplier as,

$$V_{out}=-(2k_nR)V_{id1}.Vi_{d2} \quad .....(3.8)$$

From (3.8) we see that the offsets disappear and note that the gain of this multiplier depends on the value of the load resistor and the aspect ratio of NMOS devices used in combiner cell. Hence, we obtain a new four-quadrant analog multiplier which gives the multiplied output for differential inputs V_{id1} & Vi_{d2}.

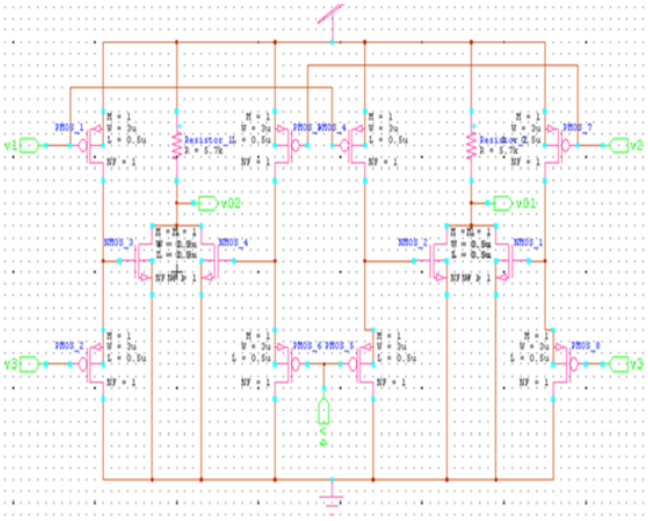
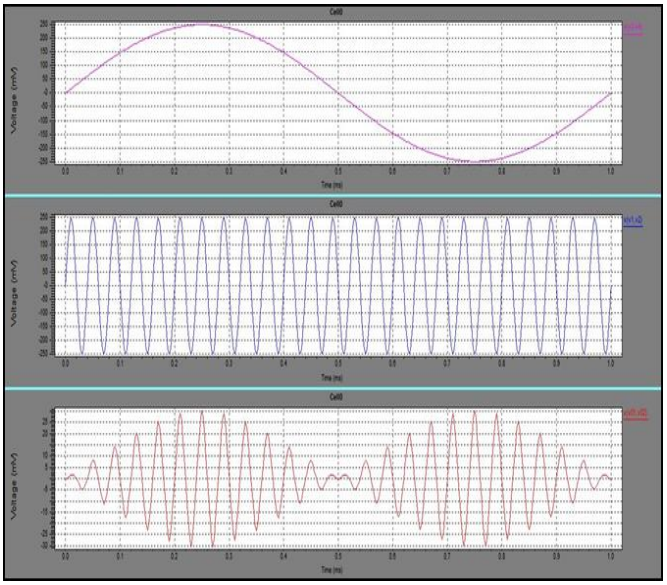


Figure 3.3 Basic Multiplier

3. Simulation Result



V_1 =0.25, 25KHZ and V_2 = 0.25, 1KHZ, the amplitude modulation is obtained as above as amplitude modulation is nothing but multiplication of two input signal varying frequency.

3. CONCLUSIONS

In this paper "low power , high linearity – CMOS analog multiplier ",the multiplier circuit is implemented in 0.35 micron technology with minimum transistor and simulated using S-EDIT and TSPICE .The power consumption avg_power 1.1138e-003.

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