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Crosstalk Delay Analysis in Very Deep Submicron VLSI Circuits

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Abstract - *The evolution of Integrated Circuit designing has been a real game changer in the field of VLSI system in the past quarter century. Very deep sub-micron (VDSM) technologies embracing sub-100nm wafer design technologies, to take advantage of the superior integration possibilities. At these technologies, many phenomena affect gate, path delay or wire delays.*

Now a days, crosstalk noise or crosstalk delay has become a challenging design issue due to growing integration density with every technology node. Since, crosstalk in interconnect had a great impact on reliability and performance of IC, that's why there is need to minimize this effect to maintain signal integrity in interconnect. In this paper, Crosstalk in proposed model can be minimized using various techniques such as buffer insertion (CMOS inverter and Schmitt trigger as a buffer), insertion along with shielding, skewing, shielding and skewing together, aspect ratio scaling and also using physical separation between interconnects.

Keywords*-aspect ratio scaling, buffer insertion, coupling capacitance, Crosstalk, CMOS buffer, Schmitt trigger,signal integrity,shielding.*

1.INTRODUCTION

Jack Kilby (a Texas Instruments engineer) in 1951 was invented Integrated circuit. Gorge Moole gave his great contribution towards integrated circuit design. As Per Moore's law, the total number of transistors on a single integrated circuit doubles every 18 months. This migration starts from few hundreds of transistor on a single chip to millions of transistor on a single chip.This migration is possible due to decrease in feature sizes of CMOS means Complementary Metal Oxide Semiconductor field effect transistor. This feature sizes changes from few micrometers to few nanometers.[1]

VLSI integrated circuit design have entered new technology termed as "Very Deep Sub-Micron" (VDSM) design technology. The design, below the feature size 0.25µm (micro-meter) fall into this category. It follows role of signal integrity, which is the ability of a signal to generate the correct response in a circuit.

Major issues concerning signal integrity are Crosstalk Delay, Crosstalk Noise, Ringing & Ground bounce, IR (voltage) drop in power lines, Electro-migration, etc.

Crosstalk delay and crosstalk noise are the primary effects which is caused due to increased coupling capacitance. Due to small and narrow feature sizes the coupling capacitance tends to be more significant.

Coupling capacitance is the main reason for crosstalk noise which occurred between two aggressor lines. In submicron designs the increase of integration density has helped to the greater proximity of adjacent wires with higher aspect ratio, thus it results in an increase in effect such as crosstalk noise and delay. [1]

Crosstalk is the interaction between signals on two different interconnects. One interconnect which is creating a crosstalk is called an "aggressor", and the one who receives this effect is called a "victim". Often, a wire can be an aggressor as well as a victim.

The RC delay of interconnect should be reduced so as to increase operating speed of an IC. Major components used to form crosstalk noise are coupling capacitance and mutual inductance.[5] Crosstalk due to coupling capacitance affects both delay and signal integrity. It is highly sensitive to spacing. Proper wire sizing and spacing, increasing driver size of victim, decreasing driver size of aggressor buffering, shielding may used to reduce coupling capacitance. whereas inductive crosstalk is globalized also affects both delay and signal integrity. shielding, buffering can be used to reduce this type of coupling.[11]

2.BACKGROUND

2.1 Subthreshold operation of a MOSFET

While considering operation of MOSFET in subthreshold region, even when transistors are normally OFF, they leak small amounts of current.

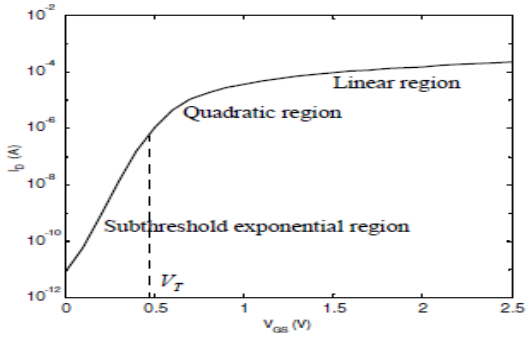

Fig.1: Id current vs. Vgs (on logarithmic scale), showing the exponential characteristic of the subthreshold region n [7].

In MOSFET Leakage mechanisms include subthreshold conduction between source and drain, gate leakage from gate to substrate and junction leakage from source to substrate and drain to substrate. Subthreshold conduction is caused by thermal emission of carriers over the potential barrier set by threshold voltage. Gate leakage is a quantum-mechanical effect caused by tunnelling through the extremely thin gate dielectric. Junction leakage is caused by current through the p-n junction between source/drain diffusions and the body.[8]

The long channel I-V model considers current only flows from source to drain when $V_{gs}>V_t$. In MOSFET, current does not cut off below threshold, but rather drops off exponentially. When the gate voltage is high, the transistor strongly ON.[7] When the gate falls below V_t, the exponential decline in current appears as a straight line on logarithmic scale. This regime of Vgs <Vt is called weak inversion. The subthreshold leakage current increases significantly with drain to source voltage i.e. Vgs because drain induced barrier lowering. In the absence of a conducting channel, the *n*+ (source) - *p* (bulk) - *n*+ (drain) terminals actually form a parasitic bipolar transistor.[8]

$$I_d = I_s . e^{Vgs/(\eta.kT/q)}(1-e^{(-Vds)/(kT/q)}) \quad \text{.....eq.1}$$

The (inverse) rate of decline of the current with respect to Vgs below Vt hence is a quality measure of a device. It is termed as the slope factor S, which measures by how much *VGS* has to be reduced for the drain current to drop by a factor of 10. [7]Hence we find,

$$S = \eta(kT/q) . \ln(10) \quad \text{.....eq.2}$$

with S is expressed in mV/decade.

2.2 Various techniques to reduce crosstalk noise

Several techniques can be used to mitigate the effects of crosstalk , some of them is as follows:

Repeater insertion is used to reduce the length of the long interconnect coupling capacitance and mutual inductance between aggressor lines also used to reduce line resistance. As switching direction changes crosstalk noise reduces at victim lines. Repeater is used to reduce power and area.

Sizing the buffer driver also used to reduce crosstalk effect.If driver size is large then conductance of driver increases. For the victim line, by increasing the driver conductance. Larger driver can be used to maintain victim line at constant voltage. For the aggressor line, using the smaller driver decreases the crosstalk noise. Proper sizing of the driver on the aggressor and victim lines used to produce lower crosstalk noise.[9]

coupling and mutual coupling can be reduced by inserting shield between aggressor and victim lines. Shield insertion used to reduce the mutual inductances due to which current return path formed by inserted shield line between both interconnect lines. Shielding is one of the effective and common ways to reduce crosstalk noise and signal delay uncertainty. Shield is nothing but a wire directly connected to vdd or gnd. One of the effective method of shielding is placing ground or power lines between two wires to reduce noise. Different parameters which can be considered while using shield are shield width, shield length, separation between shield and the signal and the number of ground connections tieing the shield to ground on the crosstalk .

Skewing is the method used to reduce crosstalk using time. Time or timing skew has been previously used in buses, where the delay of a coupled bus was reduced by skewing the timing of adjacent wires or interconnects. Skewing was applied to reduce the energy dissipation and delay of a coupled bus and was used to reduce bus peak power .

Crosstalk can be minimized using shielding and skewing technique together. It is more effective technique as compared to shielding and skewing.[5]

Schmitt trigger as a buffer is designed to operate at a higher frequency. It is used to reduce power and delay in interconnects. In comparison with conventional CMOS inverter as a buffer, buffer using Schmitt trigger switches fastly, thus it leads to the reduction in delay. Coupling noise is reduced by simultaneous buffer and

wire sizing. In order to propagate the signal with the reduced noise and delay.

Increasing the physical distance between the aggressor and victim lines can reduce the coupling capacitance and mutual inductance between two adjacent lines. Reduction in crosstalk capacitance is inversely proportional with increase in spacing.

Study of aspect ratio scaling is used to study the effect of spacing between two wires (pitch) on crosstalk where aspect ratio is ratio of width and pitch (spacing + width).When Pitch increases the difference between rise time and fall time decreases.

3. RELATED WORK

3.1 Effect of crosstalk on various interconnects parameters.

In Cu equivalent model as shown in above figure the interconnect which produces crosstalk termed as aggressor line and interconnect which is affected by crosstalk is termed as victim. To study the effect of crosstalk on various parameters such as delay, power delay product (pdp), RLC power we have simulated test setup using hspice as shown in fig.2[1]

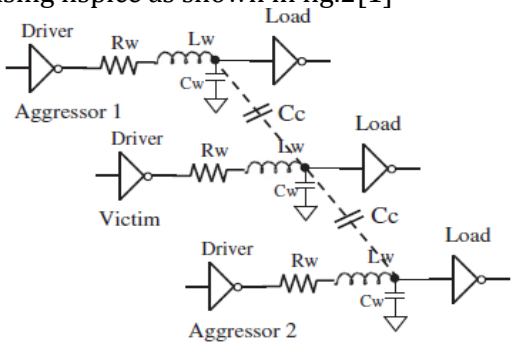

Fig.2 Cu equivalent model using RLC interconnect.[1]

Following graph shows effect of delay on length and effect of power with respect to voltage for both RC and RLC Cu equivalent model. There is increase in delay as frequency and length increases. Power consumption is better as voltage level increases.

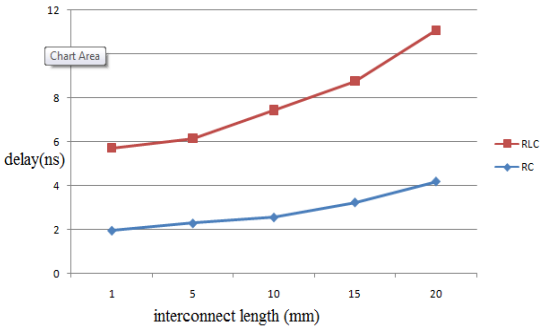

Fig.4 Effect of delay on interconnect length

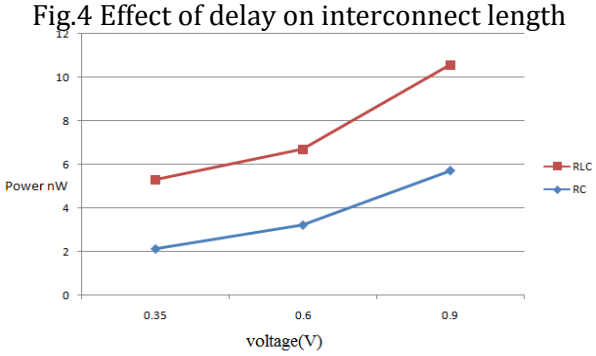

Fig.5 Effect of power on voltage

3.2 Crosstalk minimization using shielding, skewing, shielding and skewing together

To minimize Crosstalk effect shielding and skewing techniques is also used.Inserting shield between two interconnects means connecting its nodes either to Vdd or GND. Skewing is the technique, used by inserting delay in pulse. Due to which switching time is varied and it hence reduces power.

3.3 Effect of crosstalk using buffer insertion as a CMOS inverter (conventional) and Schmitt trigger.

Analysis is being processed on Schmitt trigger as a buffer which is designed to operate at a higher frequency with higher transmission rate. It is helpful to reduce delay and power as compared to conventional CMOS inverter.

In comparison with conventional CMOS buffer, a Schmitt trigger as a buffer switches fastly. Thus it leads to the reduction in delay also power. Work is being processed on designing of Schmitt trigger a buffer and CMOS inverter using hspice simulation which is operating at higher frequency like 10GHz.[5]

4. CONCLUSION

This paper concluded that Crosstalk can be minimized using various techniques such as buffer insertion like

CMOS inverter and Schmitt trigger, shield insertion, skewing, shielding and skewing together, aspect ratio scaling. But Crosstalk cannot be minimized totally.

Due to shielding capacitive load is increases that's why it is not suitable for subthreshold operation. Instead of using shield if we increases physical spacing between two interconnects or by aspect ratio scaling then there is a greater possibilities to reduce crosstalk noise and delay. It is best suitable for subthreshold operation

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