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FPGA Based Error Detection And Correction System Using Reed-Solomon Code

Vishal Chandale[#1], Pallavi Gavali[#2], Payal Giri[#3], Mrs. Anjali Shrivastav[#4]

Dept. of Electronics and Telecommunication
Pimpri Chinchwad College of Engineering, Nigdi, Pune 411044
University of Pune, India

Abstract: *Encoding and decoding are very important blocks in Communication .There are many techniques to implement Error Detection and Correction Code (EDAC), like Bose Chaudhuri-Hocquenghem (BCH) and Reed-Solomon (RS) codes . These codes can cope with multiple faults, and are based on finite-field arithmetic, also known as Galois Field . BCH codes can correct a given number of bits at any position, whereas RS codes group the bits in blocks to correct them afterwards. RS is a very popular error correcting code, and has been applied to several situations, especially in communication systems. Therefore an efficient error control code is needed to protect the digital data. In high speed communication system Reed-Solomon codes are widely used to provide error protection especially against the burst errors.*

This is project aims at designing RS encoder and decoder. The RS (n ,k) is chosen as (23,19).This is standard block code which is widely popular in communication .The encoder takes 19 bytes date block and generate 23 byte code block to be transmitted on digital communication channel .This code defines Galois Field GF(2^5) and has the capability of correcting up to 2 short bursts of errors.
The encoder and decoder coding is done in VHDL on Xilinx tool .This process is implemented on Xilinx Spartan FPGA.

1.INTRODUCTION

Communication *is* simply the act of transferring information from one place to another.
Encoding and decoding are very important blocks in Communication.
Many digital signalling applications in broadcasting use forward error correction (FEC), a technique in which redundant information is added to the signal to allow the receiver to detect and correct errors that may have occurred in transmission.

There are many techniques for error detection and correction

1. Hamming code
2. Turbo code
3. BCH code
4. Reed-solomon code

One way to compare algorithms is to compare their performance in terms of how quickly they solve the problem. Some algorithms arrive at the solution faster than others. Often the preference is towards the fastest algorithm when solving a problem. The performance of the algorithms can be measured in two different ways . It can be done by calculating the execution time (known as time complexity) and the space/ memory requirement (known as space complexity).

Reed-Solomon codes have proved to be a good compromise between efficiency and complexity. RS is a very popular error correcting code, and has been applied to several situations, especially in communication systems. Therefore an efficient error control code is needed to protect the digital data. In high speed communication system Reed-Solomon codes are

widely used to provide error protection especially against the burst errors.

2.REED SOLOMON CODE

RS codes are linear block codes and a subset of BCH codes. An RS code is based on finite fields, often called Galois fields. The number and types of errors that can be corrected depends on the characteristics of the Reed-Solomon code. RS (n, k) codes parameters are described as follows.

I. m - Number of bits per symbol

II. k- Un-coded message length in symbols

III. n- Codeword length in symbols

IV. (n-k)- Number of parity check symbols

V. t -Number of correctable symbol errors and
$2t = = n-k$

In this project (23, 19) Reed-Solomon encoders/decoders is being implemented using FPGA.

2.1STUDY OF RS CODING

2.1.1RS ENCODING

RS stands for Reed-Solomon codes.RS codes is important error-correcting codes that were introduced by Irving S. Reed and Gustave Solomon in 1960. In coding theory, the Reed–Solomon code belongs to the class of non-binary cyclic error-correcting codes. Reed–Solomon coding is very widely used in mass storage systems to correct the burst errors associated with media defects.Error detection and correction or error control are techniques that enable reliable delivery of digital data over unreliable communication channels. Many communication channels are subject to channel noise, and thus errors may be introduced during transmission from the source to a receiver. Error detection techniques allow detecting such errors, while error correction enables reconstruction of the original data in many cases.

RS coding consists of two main blocks encoder block and decoder block. In encoding block message single is converted in cypher text for the safety of data or message and then through channel it get transmiited to decoder block which decode the message signal into its originals

BLOCK DIAGRAM

Block diagram of RS code consist of two main block encoder block and decoder block

1.ENCODER

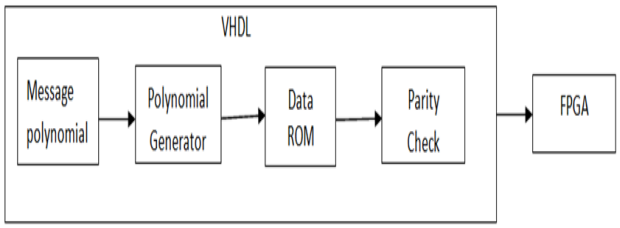

Fig-1

Block Diagram of RS Encoder

2.DECODER

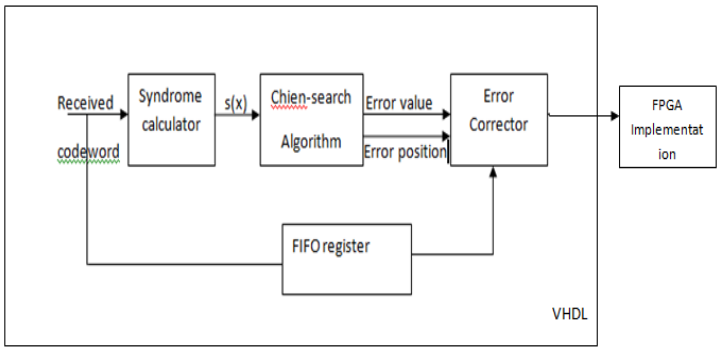

Fig. 2 Block Diagram of RS Decoder

BLOCK DIAGRAM DESCRIPTION

ENCODER BLOCK

RS codes are encoded by simply adding the parity symbols at the end of k-symbols message block which is together called as codeword and is shown in figure. At the encoder side, the information is shifted into the left

most bits by multiplying by X2t, leaving a codeword of the form,

$$C(X) = X2t\ m(x) + p(x)$$

Where C(x) is the codeword polynomial, m(X) is message polynomial and p(x) is the redundant polynomial. The parity symbol is the remainder which is obtained by dividing message block with the generator polynomial and it is represented as,

$$p(X) = (X2t\ m(X))\ mod\ g(X)$$

So, generator polynomial is responsible for generating RS codeword, which has a unique property that all valid codewords are exactly divisible by the generator polynomial. The generator polynomial is shown as,

$$G(X) = (X+\alpha)(X+\alpha2)(X+\alpha3)\ldots(X+\alpha2t)$$

$$= g0 + g1X + g2X2 + \ldots + g2t\text{-}1X2t\text{-}1 + X2t$$

where α is a primitive element in GF(2m), and g0,g1,g2, ... g2t-1 are the coefficients from GF(2m).

Elements of RS Encoder Block Diagram:

1) Message Polynomial

2) Polynomial Generator

3) Data ROM

4) Parity Check

Block Diagram Explanation of RS Encoder:

1) Message Polynomial: It is input polynomial denoted by m(x)

2) Polynomial generator: Generator polynomial is responsible for generating RS codeword, which has a unique property that all valid code words are exactly divisible by the generator polynomial. The generator polynomial is shown as,

$$G(X) = (X+\alpha)(X+\alpha2)(X+\alpha3)\ldots(X+\alpha2t) = g0 + g1X + g2X2 + \ldots + g2t\text{-}1X2t\text{-}1 + X2t$$

where α is a primitive element in GF(2m), and g0,g1,g2, ... g2t-1 are the coefficients from GF(2m).

3) Data Rom: We provide ROM to encode the message.

4) Parity Check: A **parity check** is a bit added to the end of a string of message polynomial that indicates whether the number of bits in the string with the value one is even or odd. **Parity** bits are used as the simplest form of error detecting code. There are two variants of **parity** bits: even **parity** bit and odd **parity** bit.By shifting message polynomial m(x), which is to be encoded

Simulation Result of RS Encoder:

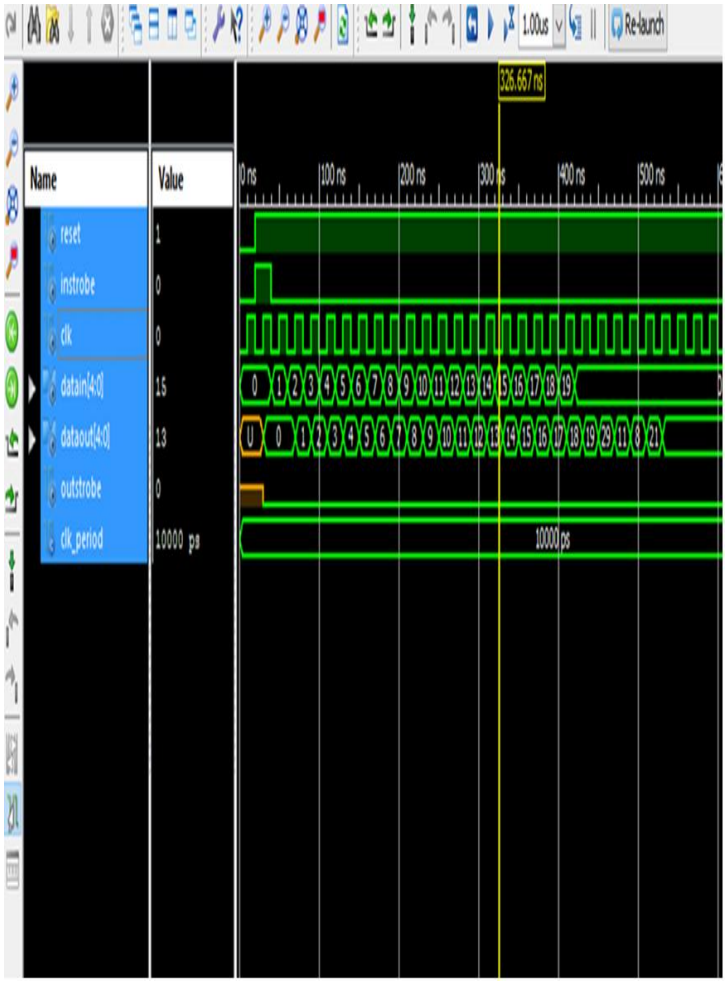

Fig-3 simulation result of rs encoder

2.1.2 RS decoding

1. Syndrome Generator: Syndrome generation from received codeword is the first step of decoding process. Here the syndromes are calculated and it is decided whether there are errors in the received codeword or not.

2. Key equation solver: The Key equation solver (KES) block provides two polynomial - error locator polynomial and error magnitude polynomial which calculates the error location and magnitude

3. Chien search: The Chien-search algorithm is used for evaluating the error position. The roots of the error locator polynomial are the inverse error locations of the codeword. This algorithm uses all possible input values and then checks to see if the outputs are zero. The sum for the odd values (σ1, σ3, σ5……) is calculated in one side and the sum for the even values (σ0, σ2, σ4, σ6,...) is calculated in other . Then the two sums are added. If the value of the summation is zero in any clock cycle (<n) then the position of the clock cycle will determine the error position.

4. Forney algorithm: Forney algorithm is used for evaluating the error values. The error position and the coefficients of ω(x) is taken here as the input. It is also using Galois field multiplier as the Chien-search algorithm.

5. Error Correction: Once the error locations and magnitudes are calculated, the error corrector block takes the received code and performs XOR operation with the corresponding error magnitudes, computed at the respective error locations to obtain the corrected message symbols. Because the error symbols are generated in the reverse order of the received codeword, a FIFO register must be applied to either the received codeword or the error vector to match the order of the bytes in both vectors. The output of XOR gate is the decoder's estimated codeword.

Simulation Result of RS decoder:

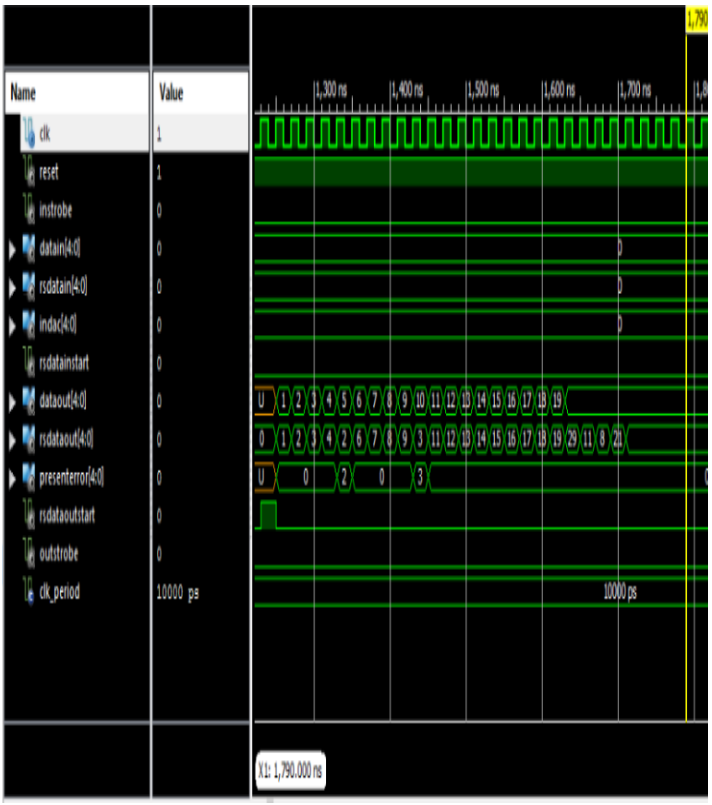

Fig-4 simulation result of rs encoder

3.HARDWARE IMPLEMENTATION

Spartan 6 FPGA

4.SOFTWARE IMPLEMENTATION

In this project we used XILINX 14.1 ISE Tool

5.CONCLUSION

Reed Solomon (23, 19) code was simulated in VHDL in Xilinx 14.1 and implemented on FPGA Sparten-6. It was found that if the error is in parity symbols even then the decoder is able to detect the output and it is of no matter to the decoder that in which symbols the error is present. The decoder first corrects the symbols and then removes the redundant parity symbols from the code word and produces the original input code word.

The encoder takes 19 bytes date block and generate 23 byte code block to be transmitted on digital communication channel .This code defines Galois Field GF(2^5) and has the capability of detecting 4 errors and correcting up to 2 short bursts of errors. Hence this is proved in simulation result.

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