DESIGN OF HYBRID PARALLEL PREFIX ADDERS

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***Abstract* — In this paper, hybrid parallel prefix adders are implemented which uses the residue number systems of reverse converters. The parallel prefix adders provide high speed but consume more power. So, hybrid parallel prefix adders are introduced which uses the modulo addition and consumes less power. These hybrid adders are implemented using parallel prefix structures.**

***Index Terms*— parallel prefix, adders, residue number system, power, hybrid adders.**

I. INTRODUCTION

In the recent years, the rapid growth of wireless communication and the handheld portable devices leads to demand on performance, cost, time to market and power. The battery powered devices requires high performance and low power consumption. So, there is need for the systems that computes fast operations and make use of power efficiently. The residue number system plays a significant role in battery based devices as it consumes less power and delay. Residue number system (RNS) is a non-weighted system which uses the residues of the number. The Residue number system consists of

1. Moduli set selection
2. Forward converter.
3. Arithmetic unit
4. Reverse converter.

Arithmetic operations on residues is done in parallel on every moduli without carry propagation between them. i.e. the RNS provides carry free operation which enhances the speed of operation and consumes low power. The RNS can also be applied in discrete Fourier transforms, fast number theoretic operations, image processing and digital signal processing (DSP) etc.

The basis for the RNS is a set of pair wise prime integers called the moduli set and the performance depends on the set that is chosen. In RNS an integer is divided into a set of smaller integers which is processed individually and parallel. The forward converter consists of binary to residue conversion and the reverse converter consists of residue to binary conversion.

II. PARALLEL PREFIX ADDERS

The main disadvantage of conventional adders is delay. Parallel prefix adders operation is based on carry look ahead adders. So, it performs with high speed computation. These adders execute the operation in parallel by decomposing into smaller pieces and the outcome of operation depends on initial inputs.

The parallel prefix operation is done in 3 stages. i.e. pre processing stage, calculation of carries, post processing stage.

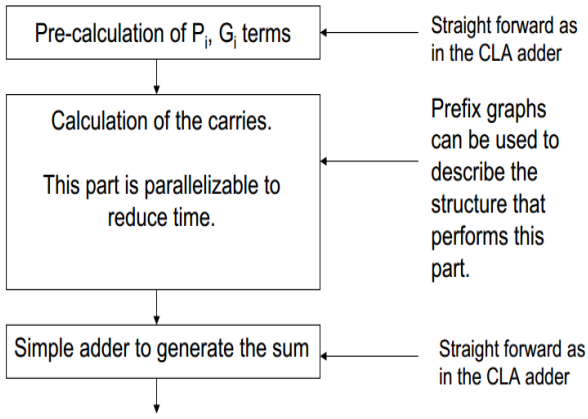


Fig 1 Parallel prefix adder operation

In the pre calculation stage propagate and generate terms are calculated.

i.e. Pi= ai xor bi
gi= ai and bi

The calculated values are passed to next stage i.e. calculation of carries. In this the components are seen in the prefix graph.

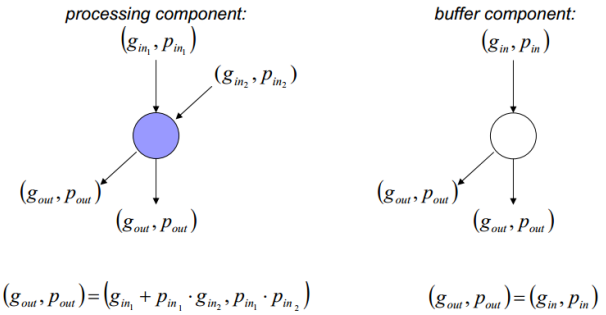


Fig 2 Carry calculation of parallel prefix adder

The execution is done in parallel by decomposing into smaller pieces. The combining operator consists of two AND gates and the OR gate. Each vertical stage produces respective propagate and generate values.

G2 = G1 OR (G0 AND P1)
P2 = P1 AND P0

The calculated carry values are forwarded to the post processing stage. In this stage the final sum values are calculated.

Sn =Pn XOR Cin

There are many types of parallel prefix adders. Some of them are

- J.Sklansky – conditional adder.
- Ladner- Fisher adder.
- Kogge- Stone adder.
- Brent- Kung adder.
- Han Carlson adder.

KOGGE –STONE ADDER

One of the parallel prefix adder is kogge stone adder. Kogge stone adder is used for high speed applications but it consumes more area. The wiring in carry calculation stage is more. The delay of this structure is $\log_2 n$. This structure faces a problem with fan-out as it uses recursive algorithm.

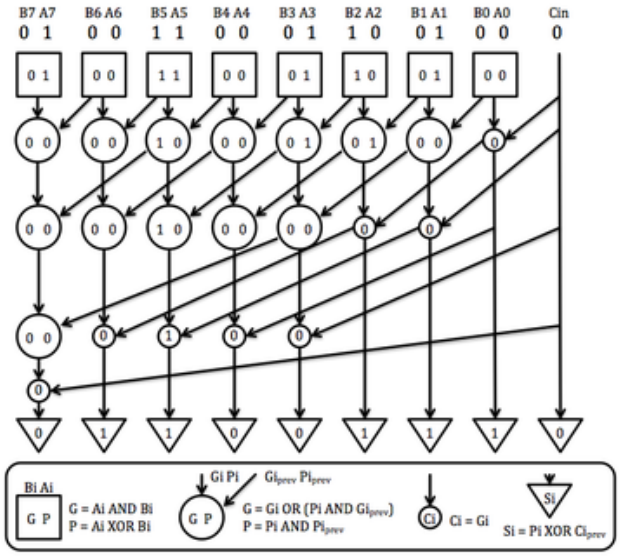


Fig 3 Kogge Stone adder

BRENT KUNG ADDER

Brent kung adder is for high speed applications with low power consumption. Its fan-out is minimum when compared to other parallel prefix adders, as it uses less wiring. The delay for this structure is [2log2]. The BK adder compute prefixes for 2 bit groups.

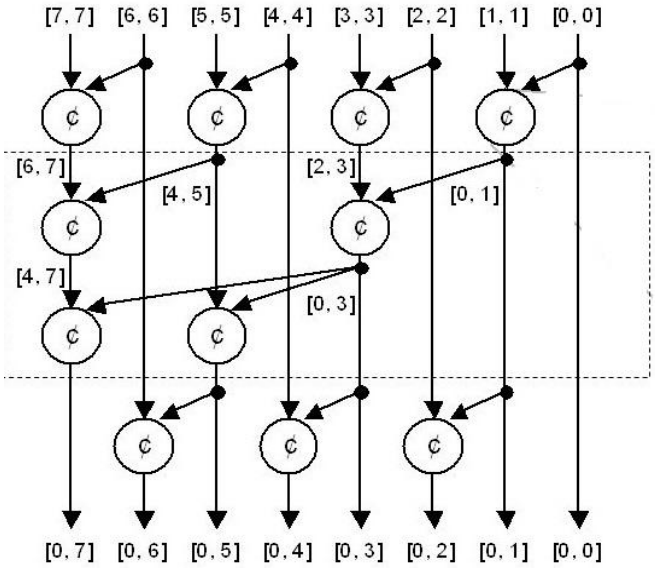


Fig 4:Brent Kung adder

III. REVERSE CONVERTER HYBRID STRUCTURES

As the reverse converter involves the conversion of residue numbers to binary, it contains complex and non modular structure. Parallel prefix adders are not suitable

for reverse converters as these adders consume more power. So, the hybrid adders are used in reverse converters which use the parallel prefix adders. In reverse converters, several parallel prefix adders can be incorporated.

HRPX BK STRUCTURE

Hybrid regular parallel prefix XNOR/OR performs the binary addition with the BK adder in the first part and in the second part of addition, simplified logic with RCA is used

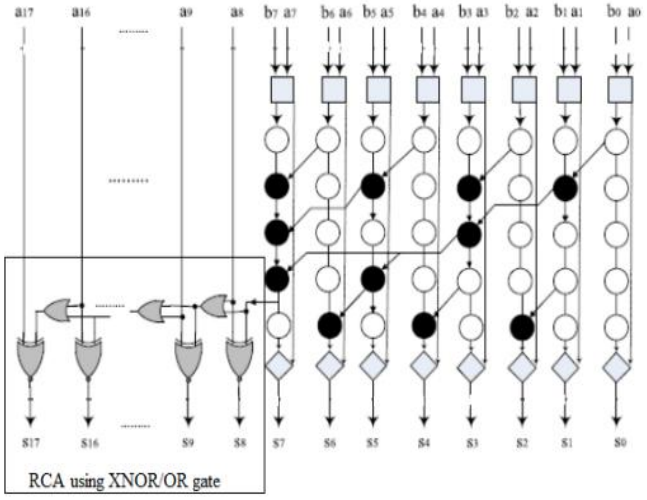


Fig 5: HRPX with BK

The full adders are replaced with XOR/OR gates. The HRPX adder performs the (4n+1) addition where n=4. The carry propagate adder with end around carry(EAC) produces double zero representation with a moduli 2n-1 adder. In reverse converters single zero representation is sufficient. So, a detector is needed for this representation which increases the delay.

HMPE BK STRUCTURE

Hybrid modular parallel prefix excess-1 structure resolves the double zero representation. The HMPE structure contains two units : Regular prefix adder and the excess-1 unit.

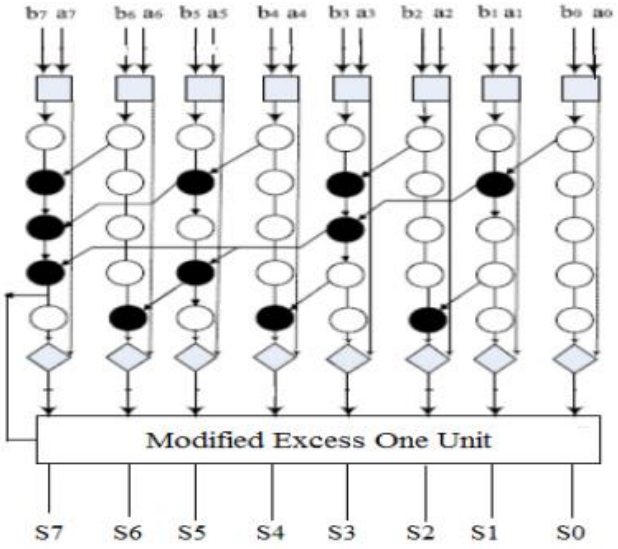


Fig 6: HMPE with BK

HMPE KS STRUCTURE

In this paper, HMPE with kogge stone adder is also designed.

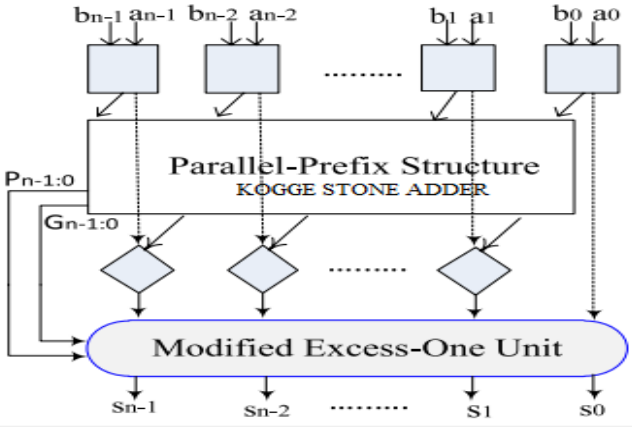


Fig 7: HMPE with KS

The result from this structure is incremented based on the control signal generated by the prefix structure. The main advantage of the excess -1 unit contains less number of logic gates compared to n bit full adder structure.

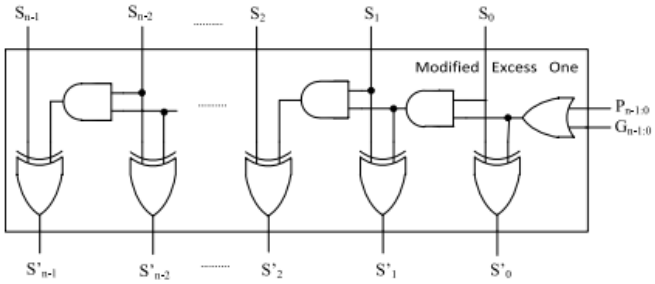
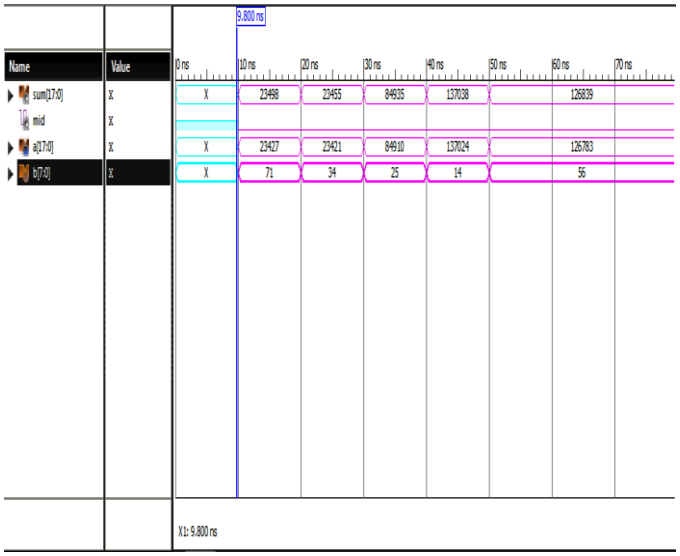


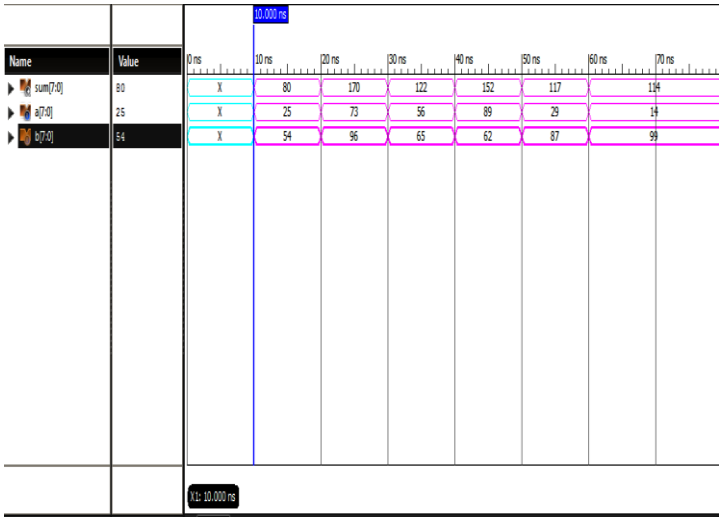
Fig 8: Excess-1 unit

III. RESULTS

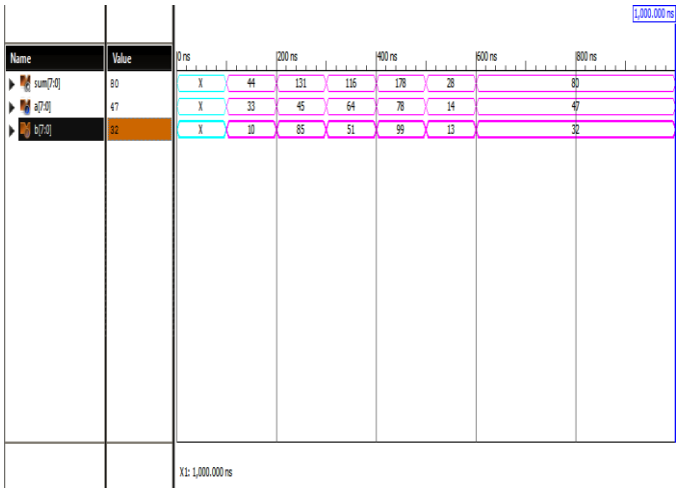
Simulation result of HRPX BK structure



Simulation result of HMPE BK structure



Simulation result of HMPE KS structure



V. CONCLUSION

Residue number system based reverse converter is designed which performs the addition for moduli sets. Parallel prefix adders are employed with the hybrid adders to achieve high speed computation and low power consumption. As a future work, the bit size can also be increased and various parallel prefix adders can also be added.

VI. REFERENCES

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