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HIGH SPEED AND LOW POWER CMOS TECHNOLOGY BASED RAM-CAM MEMORY DESIGN

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Abstract This paper presents a high speed and low power RAM-CAM memory design. Low power consumption and delay time reduction are two major goals of Content-addressable memory (CAM).The proposed SCN-CAM works at the 5v supply voltage and achieves low power and reduced delay time to that of the conventional low power CAM design.

***Key Words*: Associative memory, content-addressable memory (CAM), sparse clustered networks (SCNs), Match line (ML), Search line (SL), Match line sense amplifier (MLSA)**

1. INTRODUCTION

CONTENT-ADDRESSABLE memory (CAM) is a functional memory that contains large amounts of stored data for simultaneous comparison with the input data, and an address from among those matches of comparison is sent to the output. Search-intensive tasks that benefit from CAMs include the address lookup function in internet routers, data compression, database acceleration and neural networks [1],[2].With these applications demanding increasing CAM capacity and higher speed, the main challenge in CAM design remains that of reducing power. Due to the frequent and parallel search operations, CAMs consume a significant amount of energy. CAM architectures typically use highly capacitive search lines causing them not to be energy-efficient when scaled. For example, this power inefficiency has constrained TLBs to be limited to no more than 512 entries in current processors. Energy saving opportunities have been discovered by employing either circuit-level techniques [3], architectural-level [4], [5] techniques or the codesignof the two, [6] some of which have been surveyed in [7]. Although dynamic CMOS circuit techniques can result in low-power and low-cost CAMs, these designs can suffer from low noise-margins, charge sharing and other problems [4].A new family of associative memories based on clustered neural networks has been recently introduced [8] [9], and implemented using FPGAs [10]. Such memories make it possible to store many short messages instead of few long ones as in the conventional Hopfield neural networks [11] with significantly lower level of computational complexity.

In this we propose SCN-CAM. The CAM array is divided into several equally sized sub-blocks, which can be activated independently. For a previously trained network and given an input tag, the classifier only uses a small portion of the tag and predicts very few sub-blocks of the CAM to be activated. Once the sub-blocks are activated, the tag is compared against the few entries in them while keeping the rest deactivated and thus lowers the dynamic energy dissipation

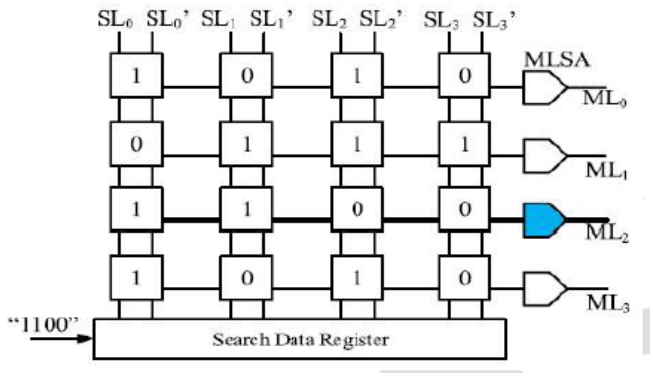

Fig -1: Typical CAM array

The circuit structure of a CAM word which is made of CAM cells. A CAM cell compares its stored bit against its corresponding search bit provided on the search-line (SL).

The combined search result for the entire word is generated on the match-line (ML). The match-line sense amplifier (MLSA) senses the state of the ML and outputs a full logic swing signal. At the circuit level, research has focused on saving power by reducing the ML and SL signal swing or using low-power current-based approaches. Even with these circuit innovations, the simple CAM circuit structure can be designed that has a very high power consumption if it is used directly to construct a large capacity CAM.

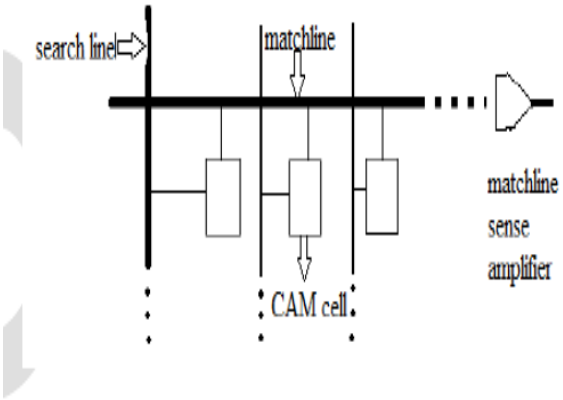

Fig -2: Circuit structure of CAM

The circuit structure of a CAM is given in the Fig1. A basic CAM cell function could be observed as twofold: bit storage as in RAM and bit comparison which is unique to CAM. At transistor i.e. circuit level CAM structure implemented as NAND-type or NOR-type. But at architectural level bit storage uses simple SRAM cell and comparison function is equivalent to XOR i.e. XNOR logic operation.

The rest of this paper is organized as follows. Section 2 describes related work. In Section 3, RAM-CAM architecture In Section 4, simulation results .Finally, conclusions are drawn in section 5.

2. RELATED WORK

Yamagata T et al [12] A 288-kb dynamic content-addressable memory cell with a stacked capacitor structure and a novel hierarchical priority encoder. Advantage is reduced circuit area, reduced power dissipation .The drawback is Alpha-particle induced soft error in dynamic cells as the storage capacitance decreases as the transistor size decreases.

Schultz K et al [13] In this content-addressable memory array is divided into B equally partitioned banks that are activated based on the value of added bits of length log2 (B) to the search data word. In this paper we find draw back that the banks can overflow since the length of the words remains the same for all the banks.

Onizawa N et al [14] A self-timed overlapped search mechanism, where mismatches can be found by searching the first few bits in a search word. Operates based on the delay of matching bits, first few bits instead of its full length a long as the consecutive sub search words are different. This paper results faster throughput than a synchronous content-addressable memory, with 38% energy saving and 8% area overhead. But the drawback is the asynchronous architecture in is more susceptible to process variations compared with its synchronous counterpart

Jarollahi H et al [15] The Sparse clustered network Content addressable memory consists of a sparse clustered network based classifier, which is connected to a special purpose content-addressable memory array. Content-addressable memory array is divided into sub blocks. Sparse clustered network based classifier connected to the content addressable memory sub-blocks gets enabled once a tag is presented, which predicts the content-addressable memory sub-blocks that are needed to be compare-enabled. The drawback is larger area overhead.

3. RAM-CAM DESIGN

First of all the system design the 6T based SRAM CMOS design. This design is to store the single bit value. This design consists of two inverter cross connection to maintain the given input data. Then the system design the 8T-xor CAM cmos design. It consists of Selection line and the bit line to control the CAM cell. This process used to find the address bit location. Then the scale based enable process is to find the CAM cell array result. The XOR- gate function to match the SRAM data and CAM data and to invert the activation result. The match line process is to check the cam data register. The clock function is to control the output matched line row then it will get the content address.

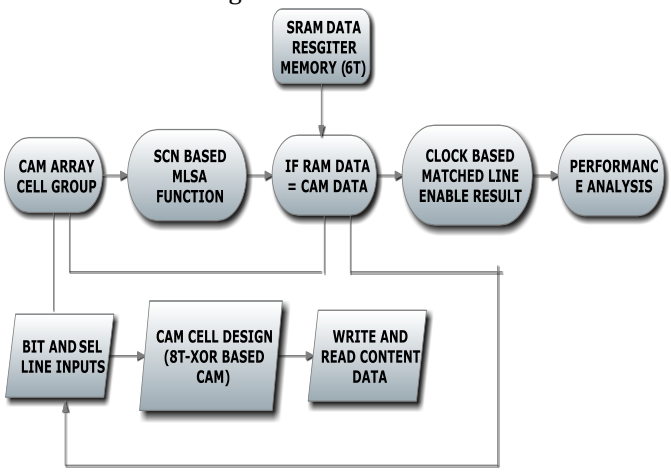

Fig -3: System Architecture

A.SRAM CMOS DESIGN

The design consists of the 6T based SRAM CMOS design. This design is to store the single bit value based on bit line and write line input. This design is to consist two inverter cross connection. This connection is to maintain the given input data. The write line is set to '1', then to get the data to cross inverter circuit connection. To design the 4-bit data register using design

B.CAM CMOS DESIGN

We design the 8T-xor CAM cmos design. This design is consist of two control line. Selection line and the bit line are control the CAM cell. This process used to find the address bit location and to check the address level and apply the evaluation logic function. It contains a CAM block that operates using self-timed control and an input controller.

C.SCAN BASED ENABLE FUNCTION

The scan based enable process is to find the CAM cell array result and to apply the cam data and ram data. The XOR- gate function to match the SRAM data and CAM data and to invert the activation result. To check the all the row cam data to data register input data bit. Then to activate the ML function.

D.ML SENSE AMPLIFIER

The match line process is to check the cam data register and ram data register value. The clock function is to control the output matched line row and to get the content address. This matched line process is mainly focused by the CAM cell array input data storage.

E.PERFORMANCE ANALYIS

The final output is to identify the content address effectively and to increase the ML check process time. Then to consider the power consumption level and to check the ml delay time also.

4. SIMULATION RESULTS

The figure 4, shows simulation result of 4*4 CAM array for voltage.

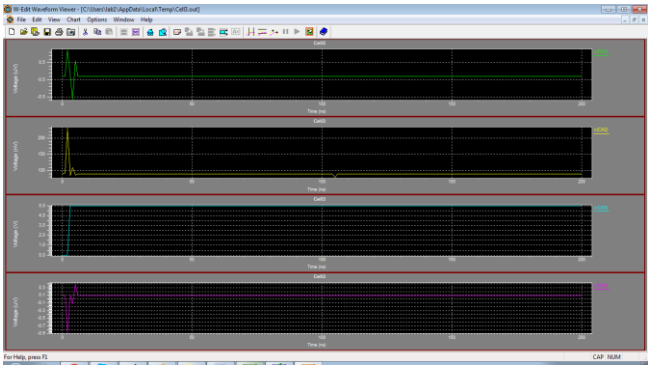

Fig -4: Simulation result for voltage

Figure 5, shows the simulation result for power. When a data is searched against the stored data .The power consumption is70mW

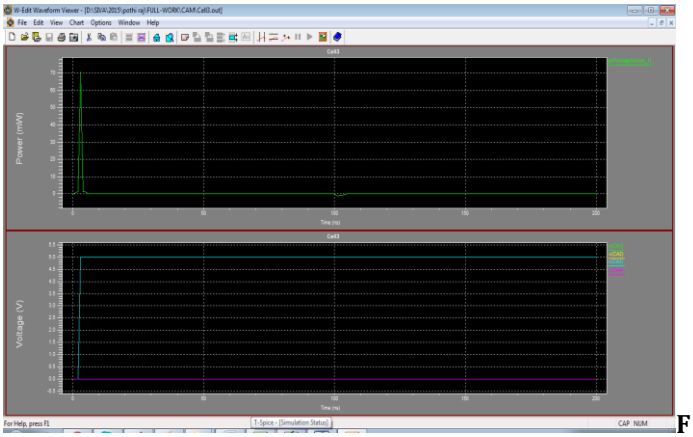

Fig -5: Simulation result for power

Table -1: Results Comparison

	EXISTING SYSTEM	PROPOSEDSYSTEM
VOLTAGE SUPPLY	1.8 V	5V
POWER	94 mW	70mW
DELAY	7ns	2.2ns

5. CONCLUSIONS

In this paper an Xor based Content addressable memory has been presented. It is a very low power CAM cell. CAM is suitable for low-power applications, where frequent and parallel look-up operations are required. In a conventional CAM array, each entry consists of a tag that, if matched with

the input, points to the location of a data word in a static random access memory block. The actual data of interest are stored in the SRAM and a tag is simply a reference to it. Therefore, when it is required to search for the data in the SRAM, it suffices to search for its corresponding tag. Consequently, the tag may be shorter than the SRAM-data and would require fewer bit comparisons. Simple and fast updates can be achieved without retraining the network entirely. Depending on the application, non-uniform inputs may result in higher power consumptions, but does not affect the accuracy of the final results

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