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Design and analysis of different types of PSK modems on FPGA for SDR

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Abstract - ***This paper presents design and analysis of different types of PSK modems on FPGA. The radio, which has many components with programmable devices, was envisioned as future of telecommunication industry. The traditional and bulky components are required to be replaced by radio, in which properties of carrier frequency, modulation, signal bandwidth and network access are defined in the software. The key requirements for SDR platform are expandability, flexibility, scalability, re-configurability and re-programmability. And in SDR the hardware usage, power consumption, configuration time plays very important role. FPGA architecture has both high speed processing capability and good reconfiguration performance, hence FPGA is a viable solution for simulation and implementation of the PSK modems. Digital Processing is a key technology for the software defined radio hardware platform. Therefore modulation and demodulation techniques have become the core of SDR technology. Digital Frequency synthesizer (DFS) is used in communication system to generate a sinusoidal carrier. The output frequency, phase and amplitude can be precisely and rapidly varied under the control of a DSP.***

Keywords: SDR, DFS, FPGA, DSP, scalability

I.INTRODUCTION TO SDR, MODEMS

SDR is a radio communication system in which the components implemented in hardware like filters, mixers, amplifiers, modulators/demodulators, detectors etc are implemented by means of software on embedded system or personal computer[1]. A basic SDR system consists of a personal computer equipped with a sound card and analog to digital converter preceded by some form of RF front end. Significant amount of signal processing is carried out by general purpose processors rather than being done in special purpose hardware. Such a system produces a radio which can receive and transmit widely different protocols or waveforms based on only the software used.

A SDR is flexible enough to avoid the limited spectrum assumptions of the designers of previous radios using software defined radios, spread spectrum technique , wireless mesh network and cognitive radio techniques. A fully implemented SDR will have the ability to navigate a wide range of frequencies with modulation techniques and programmable channel bandwidth. An Adaptive Intelligent-Software Radio (AI-SR) is capable of adapting to its environment by automatically adopting its operational mode to achieve efficiency and enhance performance. This requires the use of significant computational power, artificial intelligence to process real time adaptive algorithms

Software radios have significant utility for the military and cell phone services, both must serve a wide verity of changing real time radio protocols. The software defined radios become the dominant technology in radio communications. SDR along with software defined antennas are the cognitive radio enablers. The software defined radio platform is designed for wide range of wireless communications applications in industry, education and research. SDRs are ideal candidates to be used in multicarrier, single-band, single-carrier, multi-band and multi-mode transceivers. Commercial wireless (eg cellular, land mobile, personal communication services(PCS) etc.)Civil government (eg public safety, national

communications and local state etc.). The modulation/demodulation becomes the core of SDR technology.

A modem (modulator-demodulator) is a hardware network device that modulates one or more carrier wave signals to encode digital information for transmission and demodulates signals to decode the transmitted information. The goal is to produce a signal that can be transmitted easily and decoded to reproduce the original digital data. Modems can be used with any means of transmitting analog signals, from light emitting diodes to radio. A common type of modem is one that turns the digital data of a computer into modulated electrical signal for transmission over telephone lines and demodulated by another modem at the receiver side to recover the digital data.

Modems are generally classified by the amount of data they can send in a given unit of time, usually expressed in bits per second (symbol bit/s, sometimes abbreviated "bps"), or bytes per second (symbol B/s). Modems can also be classified by their symbol rate, measured in baud. The baud unit denotes symbols per second, or the number of times per second the modem sends a new signal. Precisely and rapidly manipulate its output frequency, amplitude, and phase under the control of a DSP compare to CORDIC Technique.

In DFS architecture extensive use of ROM is not required.Digital circuits do not suffer from the effects such as thermal drifts, component variations and aging as in analog counterparts.In case of most FPGA there exist registers in every logic cell, therefore by adding pipelined register there will not be additional hardware cost.

The wireless LAN standard IEEE8.211b uses a variety of different PSK modems depending on data rate required. Used for RFID and Blue tooth communication. BPSK is appropriate for low cost passive transmitters, biometric passports and credit cards. QPSKs are used in satellite broadcasting. GSM, CDMA, LTE, fixed and mobile wimax and cable TV applications.

II. REVIEW OF PSK MODEMS

PSK is a digital modulation scheme that conveys data by changing the phase of the reference signal. The signal is impressed into the magnetic field X, Y area by varying the sine and cosine inputs to a precise time. It is widely used for wireless LANs, Bluetooth communication and RFID. A convenient method to represent PSK scheme is on a constellation diagram.

Binary Phase reversal keying is the simplest form of phase shift keying (PSK). It uses two phases which are separated by 180° and can also be termed 2-PSK. This modulation is the robust of all the PSKs. It takes the highest level of noise or distortion to make the demodulator reach an incorrect decision. It is not suitable for high data rate applications. The π/2, phase-shift keying (π/2-BPSK) is a modulation technique which encodes the binary information in relative phase shifts of π/2 and -π/2. It has in result only two phases of the carrier, at the same frequency, but separated by 180º. DBPSK signal can be coherently demodulated or differentially demodulated. We denote the modulation scheme that uses differential encoding and differential demodulation as DBPSK.

QPSK is sometimes known as quadriphase PSK, 4-PSK or 4-QAM. QPSK uses four points on the constellation diagram, equi-spaced around a circle with four phases QPSK can encode two bits per symbol. QPSK can be used either to double the data rate compared with a BPSK system, maintaining the same Bandwidth of the signal. The π/4 QPSK modulation scheme is a modulation scheme that has combined a conventional QPSK modulation scheme with an offset QPSK (OQPSK) scheme. In π /4- QPSK, we have 8 signals, every alternate symbol is transmitted using π /4 shifted pattern of the QPSK constellation.

III.DIGITAL FREQUENCY SYNTHESIZER

Digital Frequency synthesizer is used in communication system to generate sinusoidal carrier wave [2]. DFS has an ability to tune with extremely fine frequency and phase resolution and to rapidly hop between the different frequencies.

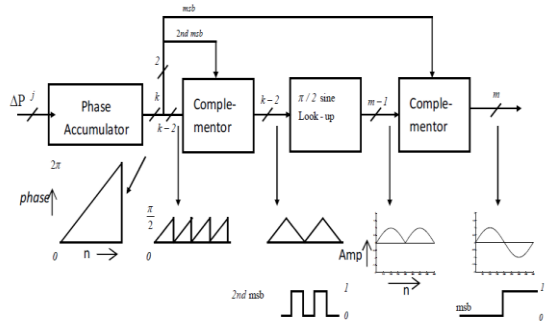

Figure 1: DFS detailed diagram

Phase Accumulator consists of a frequency register, full adder and a phase register. The digital input word (phase incremental) entered into frequency register is added to the data previously held in the phase register at each clock pulse to produce a linearly increasing phase value. By storing only π/2 radians of sine wave information compression can be achieved to generate the samples for the full 2π range in ROM. The 2 most MSB are used to decode quadrant, remaining k-2 bits are used to address a one quadrant sine look-up table. The accumulator output is used as is for the first quadrant and the bits must be complemented, so that the slope of the saw tooth is inverted for second and fourth quadrant. The sampled output at the look up table is a full wave rectified version of the desired sine wave. The final output sine wave is then generated by multiplying the -1, when the phase is between π and 2π.

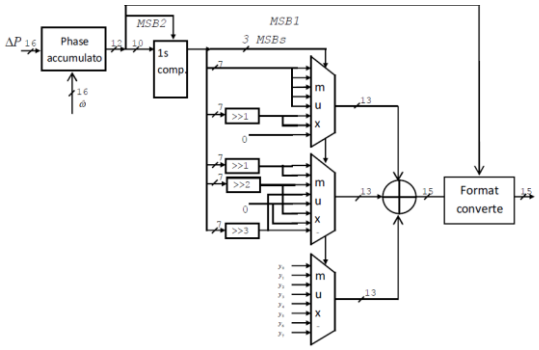

Figure 2: DFS architecture

The complete DFS architecture is shown in the figure. The phase to sine amplitude converter includes 1's complement to exploit quarter wave symmetry. The architecture is significantly less complex, does not include multiplier or squaring circuits or ROM. Only three integers need to be added to 12bits, the two MSB's are used for quadrant symmetry, next three bits identify segments. The remaining seven bits indentify different sub angles. The two upper multiplexers shift these remaining seven bits according to slopes.

IV.DESIGN OF DIFFERENT PSK MODEMS

In Binary Phase Shift keying the Digital Frequency Synthesizer architecture is implemented in verilog script to generate a sine carrier wave. The modulated signal is generated based on the binary information data bit and on the logic. If the binary information bit is 1, then the modulated signal is the sine wave, and if the data bit is 0, then the modulated signal will be the complement of the sine wave. To get the demodulated output signal the modulated signal is again compared with the reference Digital Frequency Synthesizer generated sine wave. The test bench for the Binary Phase Shift Keying-BPSK TB is written to generate BPSK modulated and demodulated waveforms.

In π/2 Binary Phase Shift keying the one Digital Frequency Synthesizer architecture is implemented in verilog script to generate a cosine carrier wave with the suitable count value. The modulated signal is generated based on the binary information data bit and on the logic. If the binary information bit is 1, then the modulated signal is the cosine wave, and if the data bit is 0, then the modulated signal will be the complement of the cosine wave. To get the demodulated output signal the modulated signal is again compared with the reference Digital Frequency Synthesizer generated cosine wave. The test bench for the π/2 Binary Phase Shift Keying-BPSK TB is written to generate BPSK modulated and demodulated waveforms.

In π/2 Differential Binary Phase Shift keying the one Digital Frequency Synthesizer architecture is implemented in verilog script to generate a sine carrier wave with the suitable count value. The modulated signal is generated based on the Ex-or of the binary information data bit and the previous bit. If the Ex-or of information bit and the previous bit is '0', then the modulated signal is the cosine wave, and if the Ex-or of information bit and

the previous bit is different data bit is '1', then the modulated signal will be the complement of the cosine wave To get the demodulated output signal the modulated signal is again compared with Previous symbol as the reference signal to get back the original signal..

In Quadrature Phase Shift keying the two Digital Frequency Synthesizer architecture is implemented in verilog script to generate a sine carrier wave with the suitable count value. The modulated signal is generated based on the binary information data di bit and on the logic. To get the demodulated output signal the modulated signal is again compared with the reference Digital Frequency Synthesizer generated sine waves.

In π /4 Quadrature Phase Shift keying the four Digital Frequency Synthesizer architecture is implemented in verilog script to generate a sine carrier wave with the suitable count value. The modulated signal is generated based on the binary information data Three bit and on the logic.To get the demodulated output signal the modulated signal is again compared with the reference Digital Frequency Synthesizer generated sine waves.

V. RESULTS AND DISCUSSION

The different types of PSK like BPSK, π/2BPSK, π/2DBPSK, QPSK and π/4QPSK are implemented in verilog script to perform both modulation and demodulation using DFS architecture. Figure shows the simulation results for all the modems.

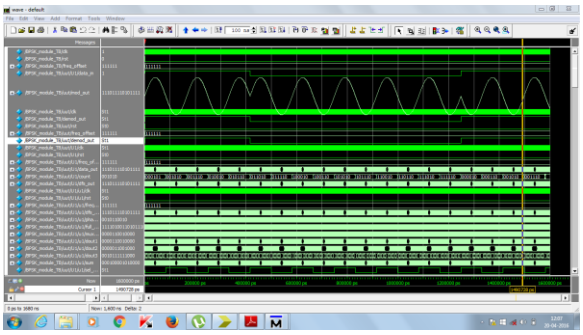

Figure 3: BPSK mod/demod waveforms

The BPSK snapshot showing the information signal is encoded with sine and complement of the sine wave and the phase difference between thw signals is 180^0.

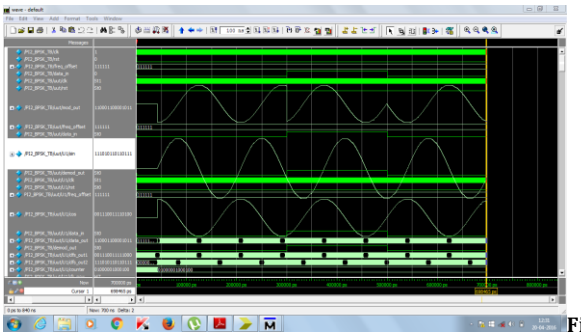

Figure 4: DBPSK mod/demod waveforms

The π/2 BPSK snapshot showing the information signal is encoded with cosine and complement of the c sine wave and the phase difference between thw signals is 90^0.

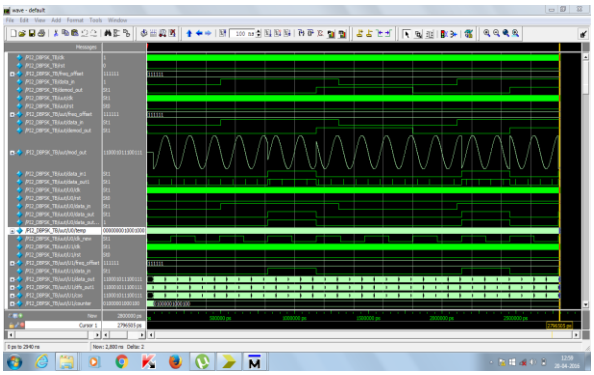

Figure 5: π /2 DBPSK mod/demod waveforms

The π/2 DBPSK snapshot showing the information signal is encoded with cosine and complement of the cosine wave based on differential encoding.

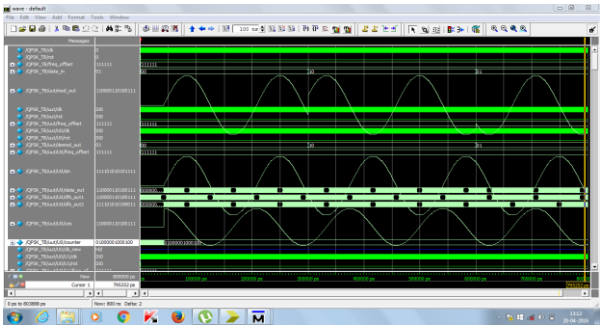

Figure 6: QPSK mod/demod waveforms

The QPSK snapshot showing the information signal is encoded with bidata bits in terms of sin and cosine waveforms and its complements.

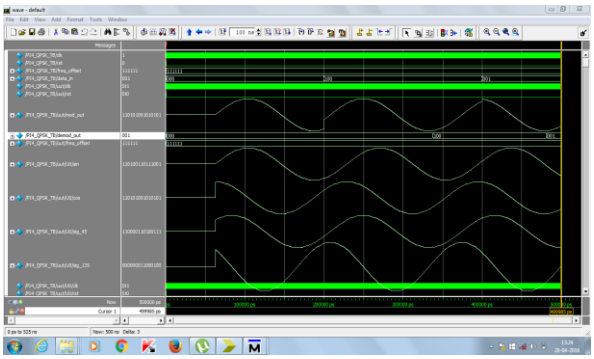

Figure 7: π /4 QPSK mod/demod waveforms

The π/4 QPSK snapshot showing the information signal is encoded with cosine, sig-45^0 and sig-135^0 waveforms and its complements to encode 3-bits /symbol for 8 combinations.

VI. CONCLUSION

The different types of PSK modems useful for satellite communication system are effectively implemented in verilog script. The sinusoidal carrier wave is generated using Digital Frequency Synthesizer, in which the Phase, amplitude and output frequency and be precisely and rapidly manipulated. And the modulation carried out using DFS architecture has a multiplier less structure utilizes less resource on FPGA.DFS has a ability to tune with extremely fine frequency and phase resolution and to rapidly jump between the frequencies. The DFS has less complex architecture compared to CORDIC.

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