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Review of Bandgap Voltage Reference for Analog and Mixed Signal Circuit

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Abstract - *This paper presents a review of the design of different bandgap reference circuits on the basis of different parameters such as V_{ref}, supply range, power dissipation, temperature coefficient etc. The proposed circuit would be a high PSRR and low temperature sensitivity and is capable of operating properly at supply voltages lower than 1V. In that circuit, the PSRR will be improved using regulated voltage and a feedback loop. In addition, the circuits will independent on supply voltage noise.*

Key Words: **Bandgap reference, High PSRR, Startup circuit, CMOS Analog Circuit Design, low Voltage**

1.INTRODUCTION

This Band gap voltage references (BGRs) are key parts of many analog and mixed signal circuits such as A/D,D/A, DRAM and flash memories. The low-power and low voltage operations are increasingly in demand for battery operated portable devices. The performance of these circuits are directly depends on BGR characteristics such as nominal voltage reference value (V_{ref}), temperature coefficient (T_C), temperature range (T_R), accuracy, consumption etc. The output generators are designed to stabilize over supply voltage, process and temperature variations. Band gap voltage reference is a reference voltage generator that can successfully achieve these requirements; it generates an output voltage equal to the silicon energy gap voltage of around 1.25V, measured in electron volts.

By definition bandgap reference is a voltage reference of which the output voltage is referred to the bandgap energy of the used semiconductor. The first bandgap reference was proposed by Robert Widlar in 1971 (2). A bandgap reference (BGR) is a basic design block of any analog circuit. The BGR generator circuit is designed to achieve the insensitive behaviour with respect to process, voltage and temperature (PVT) corners. The BGR supplies the reference voltage and the reference current to the analog design blocks such as a charge pump and a memory circuit.

1.1 Background

Bandgap voltage reference circuit is most commonly used for all analog circuits for providing reference voltages. Fig 1 illustrates the working principle of the bandgap reference circuit. In this circuit V_T increases linearly with temperature while V_{BE} decreases approximately linearly with temperature. For generating low temperature dependent reference voltage (V_{ref}), both V_{BE} and V_T are summed along with the temperature scaling (K) factor. The scaling factor is considered for positive temperature coefficient because V_{BE} changes -2 mV/°C and V_T changes 0.086 mV/.

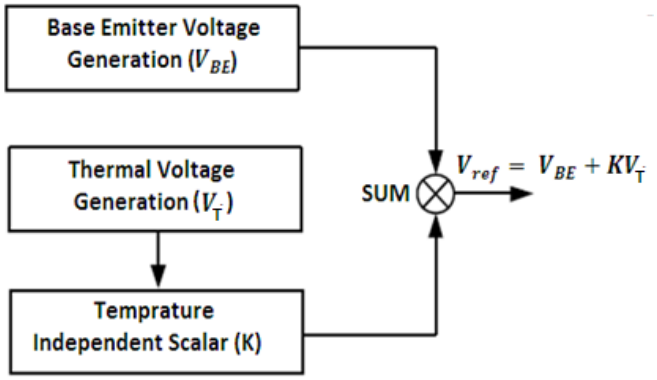

Fig -1: Principle of Bandgap reference Voltage

The working principle of the conventional bandgap reference circuit can be understood from Fig 2, which is composed of CMOS opamp, BJTs and resistors.

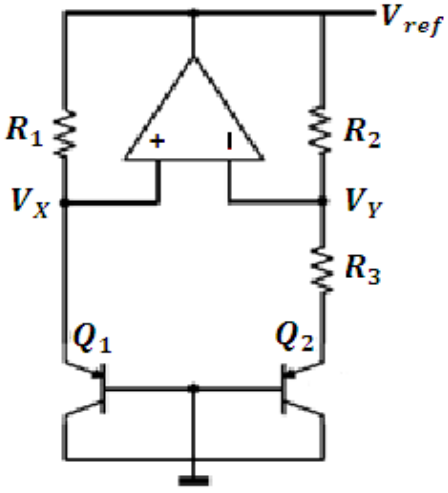

Fig -2: Conventional BGR Circuit

The relation between the diode current and V_{BE} voltage can expressed as

$$I = I_s * \left(e^{V_{BE}/V_T} - 1\right) \ (or) \ V_{BE} = V_T * \ln\frac{I}{I_s} \quad (1)$$

Where V_T =KT/q, in which K is Boltzmann's constant (1.38 * 10-23 J/K) and q is electronic charge (1.6 * 10-19 C). ΔV_{BE} is the forward voltage difference between Q1 and Q2 transistors for different current densities.

$$\Delta V_{BE} = V_T * \ln(n) \quad (2)$$

In conventional bandgap reference circuit VX and VY nodes are controlled by opamp circuit and the BGR output voltage V_{ref} is given by :

$$V_{ref} = V_{BE} + V_T * \ln(n)\,(1 + R_2/R_3) \quad (3)$$

1.2 STARTUP CIRCUIT

The transistors have two states, on and off, when power is provided. In order to make sure the circuit works properly, we need a mechanism which can provide a small current to flow through Op Amp and enable it. This mechanism is also required to be turned off when Op Amp works properly. The start-up circuit consists of transistors, M3-M5. The mechanism works as the following. Since M3 is also in saturation, it provides a sufficient gate voltage for M5 to turn on. When M5 is on, a small current will flow through Op Amp and enable the entire circuit. Furthermore, M4 will turn on and sink all the current from M3 and disable M5.
Then the start-up circuit is disabled.

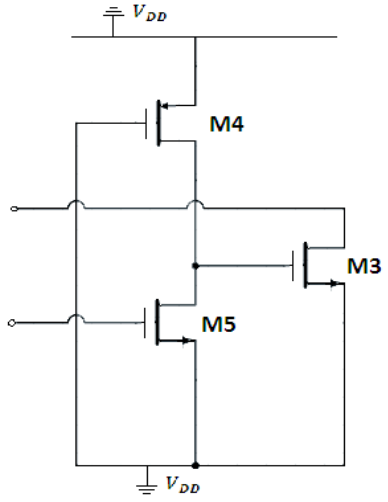

Fig -3: Startup Circuit

2. COMPARISON TABLE

Table -1:

Name of Authors	S. Mehrmanesh, M. B. Vahidfar, H. A. Aslanzadeh, M. Atarodi	Y. Yuzman, H. Che Lah, N. Razali, H. Siti Noor, Y. Tan Kong,	B.RobertGregoire& Un-Ku Moon,
Year reported	2003	2012	2012
CMOS Technology	0.25µm	0.18 µm	0.18 µm
V_{REF}	700mv	1.204 V	343 mV
Supply Range	1to 2.5v	------	1.5 to 3.5V
Power dissipation	200µW	150 µm	117 µm
Temperature coefficient	0.3%	6.1ppm/ºc	3ppm/ºc
Temperature Range	0ºC to 7ºC	-20ºC to 90ºC	-40ºC to120ºC
PSRR at DC	110db	84 dB	77 dB
PSRR at 10KHZ	100db	44 dB	77 dB
PSRR at 1MHZ	70db	20 db	68 dB
Application	Temperature compensated circuit	Analog mixed signal circuit like data converters, smart sensors and power management circuits	Analog mixed-mode circuits and digital circuit

Table -2:

Name of Authors	Jing-Hu Li, Xing-bao Zhang & Ming-yan Yu	David C. W. Ng, David K. K. Kwong & Ngai Wong
Year reported	2011	2011
CMOS Technology	0.5 µm	0.5 µm
V_{REF}	487.6 mV	228 mV
Supply Range	1.2 to 3V	1 to 5V
Power dissipation	48 µm	28 µm
Temperature coefficient	8.9ppm/ºc	34ppm/ºc
Temperature Range	-40ºC to110º C	-40ºCto120ºC
PSRR at DC	58 dB	58 dB
PSRR at 10KHZ	20 dB	58 dB
PSRR at 1MHZ	15 dB	12 dB
Application	Analog and mixed-signal applications, such as regulators, analog-to-digital(A/D) and digital-to analog converter	high-speed analog-to-digital converters (ADCs) or switched-mode power supplies (SMPSs)

3. THE PROPOSED BAND GAP VOLTAGE REFERENCE

The Gate-Source voltage of NMOS transistors depends on electron mobility and threshold Voltage, therefore

$$V_{GS} = V_{th} + \sqrt{\frac{2lI_D}{c_{ox} W \mu_n}} \quad (4)$$

Where I_D is the drain current of the transistor, W/I is the width-to-length ratio of the channel and Cox is unit capacitor of the Gate-Oxide. μ_n is the electron mobility and Vth the threshold voltage of NMOS transistor .The threshold voltage and electrons mobility dependence on temperature are given in (5) and (6).

$$\mu_n(T) = \mu_{n0}\left(\frac{T}{T_0}\right)^{\propto \mu n} \quad (5)$$

$$V_{tn} = V_{tn0} + \propto_{vtn} (T - T_0) \quad (6)$$

where $\mu_n, \propto_{\mu n}, V_{tn0}, \propto_{vtn}$ are negative constant values and $\propto_{\mu n}$, $\propto_{vtn}$ are negative constants. T_0 and T are 300 kelvin and temperature coefficient, respectively. $\propto_{\mu n}$ in equation (5) ranges between -1 and -2. Therefore, the electron's mobility is inversely proportional to temperature. Since $\propto_{vtn}$ in equation (3) is negative, threshold voltage of NMOS is inversely proportional to temperature. The Gate-Source voltage of NMOS in equation (4) is capable of varying both inversely and directly. The first term produces the inverse relationship and the produces the direct relationship with temperature in VGS.

Equation (4) shows variations of resistance with temperature. This phenomenon strongly affects both directly and inversely temperature-dependent currents in band gap voltage references and cause significant changes in the mentioned currents.
The amount of resistance in the ambient temperature (T_0) is shown as $R(T_0)$bellow, which is dependent on fabrication process. However, temperature coefficients of TC_1 and TC_2 are constant values and are independent on fabrication process.

$$R(T) = R(T_0)[1 + TC_1(T - T_0)] + TC_2(T - T_0)^2 \quad (7)$$

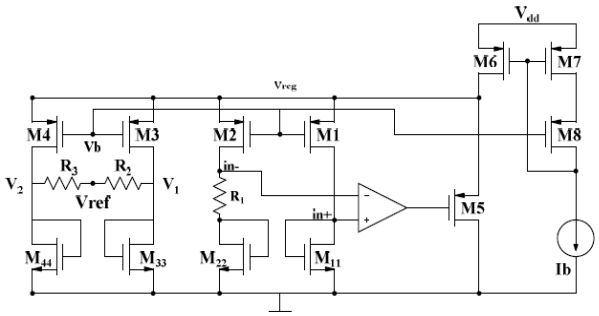

Fig -4: General schematic of proposed band gap reference

Thus, a resistor with smaller temperature coefficient is required. Consequently, unsolicited Polysilicon resistor in 90nm CMOS technology is utilized in the proposed circuit. PSRR is improved in the circuit using regulated voltage of VREG. In this structure, regulated voltage and supply voltage have been separated. In contrast with the previously suggested band gap voltage references, the required decrease in supply voltage is equal to Source-Drain voltage in M6 and M7 transistors. In continue, the structure of the proposed band gap voltage reference using diode MOSFETs in strong inversion region is demonstrated in Fig. 2. +in and –in nodes in operational amplifier are equal. The voltage acrossR1

varies with temperature according to equations (7) and (6). Temperature behavior of Gate Source voltage in diode transistors depend on the drain current and the size of the NMOS transistor.

$$V_{R1} = V_{GS11} - V_{GS22} \quad (8)$$

$$V_{R1} = V_{tn11} + \sqrt{\left(\frac{2LI_D}{C_{OX}W_{\mu n}}\right)M_{11}} - V_{tn22} - \sqrt{\left(\frac{2LI_D}{C_{OX}W_{\mu n}}\right)M_{22}} \quad (9)$$

Length and drain current of M11 and M22 of equation (9) are equal and their threshold voltages are close. Hence, equation (10) can be simplified as equation (11)

$$V_{R1} = \sqrt{\left(\frac{2LI_D}{C_{OX}W_{\mu n}}\right)M_{11}} - \sqrt{\left(\frac{2LI_D}{C_{OX}W_{\mu n}}\right)M_{22}} \quad (10)$$

VR1 in equation (7) is subtraction of two temperature-dependent terms. In order to obtain variations in voltage across R1 which is proportional to temperature, first term must be greater than the latter. Consequently, using proper values for channel length in M11 and M22 diode transistors result in proportionally temperature-dependent voltage across R1. In other words, W22must be greater than W11 and it must be W22=1.39W11

Current flowing through R1 resistor is calculated from equation (9). The current is obtained as a result of the difference in Gate-Source voltages of M11 and M22 across R1. Equation (10) suggests that the current flowing through M3 and M4 are proportional to IR1.

$$I_{R1} = \frac{V_{GS11} - V_{GS22}}{R_1} = \frac{\Delta V_{GS}}{R_1} \quad (11)$$

$$I_{M3,4} = I_{R1}\left(\frac{(W/L)_{M_{3,4}}}{(W/L)_{M_{1,2}}}\right) \quad (12)$$

Voltages of V1 and V2 nodes are the Gate-Source voltages of M33 and M44, respectively, which are diode connected in strong inversion region. The output voltages before connecting R4 and R5 are calculated from equation (12).

$$V_{ref} = \frac{V_{tn33} + \sqrt{\left(\frac{2LI_D}{C_{OX}W_{\mu n}}\right)M_{33}}}{1+(R_2/R_3)} + \frac{V_{tn44} + \sqrt{\left(\frac{2LI_D}{C_{OX}W_{\mu n}}\right)M_{44}}}{1+(R_3/R_2)} \quad (13)$$

Where channel lengths of M3 and M4 are equal and their threshold voltages are close. Therefore,
Temperature behaviour of the Gate-Source voltage is only affected by the channel width of M33 and M44. In other words, M44 must be greater than M33 and should be WM33=2.38WM44. It is obvious from (9) that IR1 has proportionate changing with temperature and bias the M3 and M4 as a current mirror with equal currents. These equal currents bias the M33 and M44 with diode connecting in strong inversion.

The (12) comprises two terms, the first one is V1 which has inverse relation with temperature $(V_{tn33} > \sqrt{\left(\frac{2LI_D}{C_{OX}W_{\mu n}}\right)M_{33}}$ and the second term is V2 which is proportional to temperature $(V_{tn44} > \sqrt{\left(\frac{2LI_D}{C_{OX}W_{\mu n}}\right)M_{44}})$
So reference voltage is:

$$V_{ref} = \frac{V_{ref}}{1+\frac{(R_2+[(\frac{1}{g_{mss}})\|(ro_{mss})])\|(R_2+[(\frac{1}{g_{mss}})\|(ro_{mss})])}{R_4+R_5}} \quad (14)$$

4. High Power Supply Rejection Ratio

The PSRR in the proposed structure is enhanced using regulated voltage of Vreg. Mirror currents in M6 and M7 transistors provide regulated voltage Vreg as power supply for the core. The current source Ib which is shown in Fig. 4 is independent from supply voltage and is a fraction of the current flowing through M1-M4. This structure separates the regulated voltage and supply voltage. This structure separates the regulated voltage from supply voltage. In comparison with the conventional band gap circuits, in this structure supply voltage required decrement is equal to the drain-source voltages of M6 and M7. In addition, M8 is biased in connection with M1-M4 in cascade configuration. The effects of supply voltage noise on regulated voltage Vreg is attenuated using following techniques.

1. Using Cascade current source configuration.
2. Utilizing a feedback loop. Feedback loop in Vreg node using a high gain op-amp amplifies the voltage difference between +in and –in nodes.

5. CONCLUSIONS

In this paper, the design of different band gap reference circuits has been reviewed. A new method for designing an low power and high PSRR band gap voltage reference for analog and mix signal circuit was proposed.

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