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COMBINATIONAL CIRCUITS USING TRANSMISSION GATE LOGIC FOR POWER OPTIMIZATION

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Abstract- *In this paper power and energy dissipation are reduced using transmission gate logic(TGL), which are the challenging factors in the VLSI CMOS design. In order to get strong output level PMOS and NMOS are connected together.In active mode, TGL technique achieves 83% power reduction as compared to the conventional CMOS design.125nm CMOS technology is used to simulate outputs in TANNER software.TGL is used in combinational circuit design to reduce complexity,leakage current and leakage power.*

I. INTRODUCTION

International Technology Roadmap for Semiconductors(ITRS) states that leakage power dissipation may ultimately dominate total power consumption as technology feature sizes shrink. During the last two decades the idea to augment the performance of logic circuits results in the progress of many logical design techniques, even though there are several process technology and circuit level solutions to reduce leakage in processors. This paper desires to bound power consumption and makes an attempt to increase eminence for transporting the signal from input to output.

II.COMBINATIONAL CIRCUITS

Combinational logic is a type of digital logic which is implemented with Boolean circuits, whose outputs is the pure function of present inputs. In contrast to sequential logic, combinational logic does not have a memory.The most important types of combinational circuit are RAM, ROM, Multiplexers, Encoders, Decoders, Demultiplexers, half adder, full adder, half subtracter,full subtracter.Combinational logic is constructed using one of the two methods; a sum of products, or a product of sums. By evasion combinational logic circuits have no memory, timing, feedback loops contained by their design. The output of combinational logic circuits is dependent on the combination of the inputs. So the change in state of one of its input condition from logic 0 to logic 1 or logic 1 to logic 0 will automatically have effect in output. To produce more complicated switching circuits the basic logic NAND, NOR and NOT are combined or connected together.

1. Combinational circuits have the following characteristics:For the combinational circuit the output at any instant of time depends only on the levels present at the input terminals.
2. There is no memory for the combinational circuit. The present state of the circuit is not affected by the previous state of the input.
3. There are n number of inputs and m number of outputs for a combinational circuit.

There is a mixture of combinational and sequential logic in practical computer circuits. For example, combinational logic is used to construct the part of the arithmetic logic unit that does mathematical calculations.

BLOCK DIAGRAM

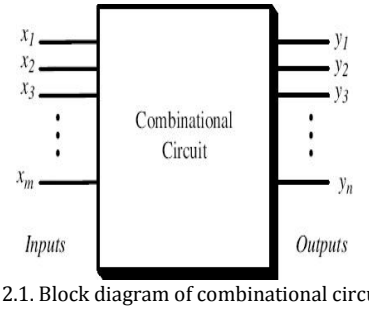

Fig. 2.1. Block diagram of combinational circuits.

III.TRANSMISSION GATE

A transmission gate can conduct in both directions or block by a control signal with almost any voltage potential analogous to that of relay. It is CMOS based switch in which PMOS passes a strong 1 but poor 0 and NMOS passes strong 0 but poor 1. Both PMOS and NMOS work simultaneously. In principle, a transmission gate made up of two field effect transistors, in which - in contrast to traditional discrete field effect transistors - the substrate terminal (Bulk) is not connected internally to the source terminal.

The two transistors, an n-channel MOSFET and a p-channel MOSFET are connected in parallel with this, however, only the drain and source terminals of the two transistors are connected together. Their gate terminals are connected to each other via a NOT gate (inverter), to form the control terminal. As with discrete transistors, the substrate terminal is connected to the source connection, so there is a transistor to the parallel diode (body diode), whereby the transistor passes backwards.

However, since a transmission gate must block flow in either direction, the substrate terminals are connected to the respective supply voltage potential in order to ensure that the substrate diode is always operated in the reverse direction. The substrate terminal of the p-channel MOSFET is thus connected to the positive supply voltage potential and the substrate terminal of the n-channel MOSFET connected to the negative supply voltage potential.

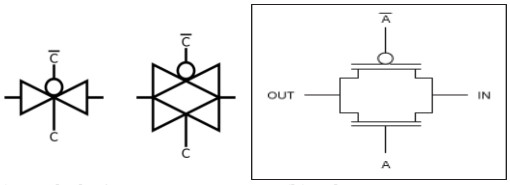

Fig.3.1(a).symbol of transmission gate, (b).schematic representation of transmission gate.

In Fig 2.1(a).when the control input is logic zero (negative power supply potential), the gate of the n-channel MOSFET is also at a negative supply voltage potential. The gate terminal of the p-channel MOSFET is caused by the inverter, to the positive supply voltage potential. Regardless of on which switching terminal of the transmission gate (A or B) a voltage is applied (within the permissible range), the gate-source voltage of the n-channel MOSFETs is always negative, and the p-channel MOSFETs is always positive. Accordingly, neither of the two transistors will conduct and the transmission gate turns off.

When the control input is a logic one, so the gate terminal of the n-channel MOSFETs is located at a positive supply voltage potential. By the inverter, the gate terminal of the p-channel MOSFETs is now at a negative supply voltage potential. As the substrate terminal of the transistors is not connected to the source terminal, the drain and source terminals are almost equal and the transistors start at a voltage difference between the gate terminal and one of these conducts.

IV. ADVANTAGES OF TRANSMISSION GATE

Logic circuits can be constructed with the aid of transmission gates instead of traditional CMOS pull-up and pull-down networks. Such circuits can often be made more compact, which can be an important consideration in silicon implementations. In a security application, they can selectively block critical signals or data from being transmitted without proper hardware-controlled authorization.

V. RULES AND DIFFICULTIES

Using complementary pairs of nMOS and pMOS devices, either the lower nMOS network is active, which ties the output to ground either the upper pMOS network is active, which ties the output to VDD. In conventional CMOS basic gates, there should exist no combination when both nMOS and pMOS networks would be ON. If this case had happened, a resistive path would be created between VDD and VSS supply rails.

The situation where neither nMOS norpMOS networks would be OFF should be also avoided, because the output would be undetermined. Series connection of transmission gates should be avoided because signal strength decreases and there occurs incorrect switching at the outputs.

VI.POWER OPTIMIZATION

Pass Transistors, Transmission Gates and Gate Diffusion Input are different techniques in design of low power digital circuits. Pass transistor design have small nodal capacitance which results in high speed. The amount of transistors used here were very low so that there is low power dissipation. Reduced number of transistors occupies small area which leads to minimize the interconnection of the wires. There are two main disadvantages with pass transistor design; one is the threshold voltage across the single channel Pass Transistor, which results in reduced drive and slow operation.

Other one was, full swing voltage at output is not possible. Another technique was, Transmission gate used to realize complex logic functions. The degradation voltage level at output problem can be overcome by using this technique.CMOS has a static power, dynamic power and delay of about 356.56pW,12.49µW and 551psrespectively whereas transmission gate has no static power and 9.4µW dynamic power and 1.39ns delay.

VII.RESULTS AND DISCUSSION

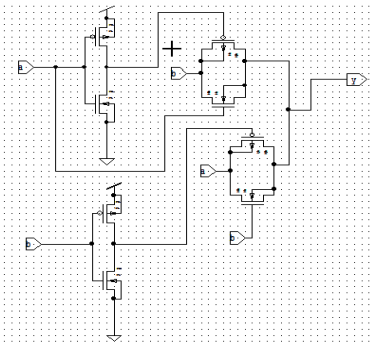

Fig. 7.1.AND gate circuit using TG

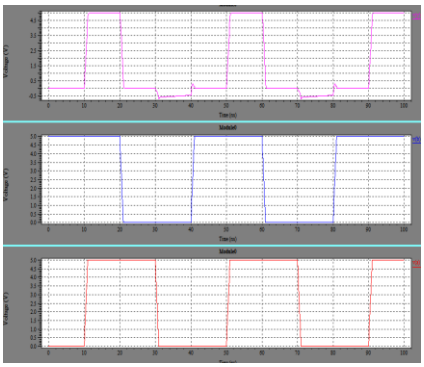

Fig.7.1.1. AND gate simulation output

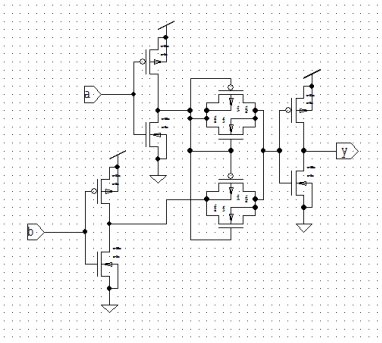

Fig.7.2.OR gate circuit using TG

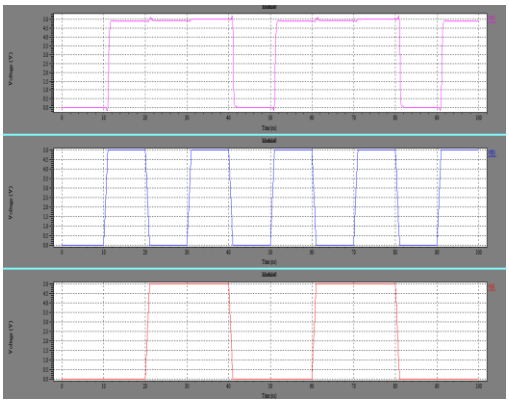

Fig.7.2.1 OR gate simulation output

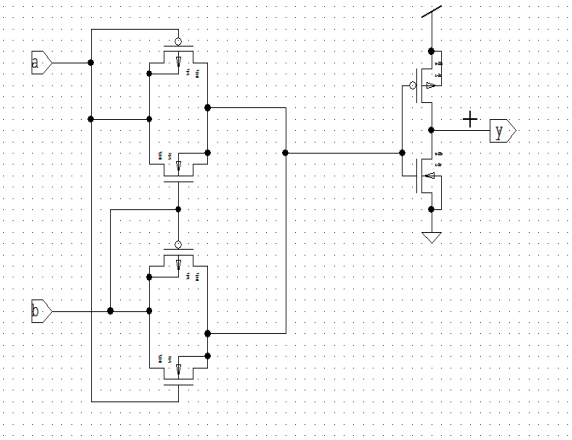

Fig.7.3.NAND gate circuit using TG

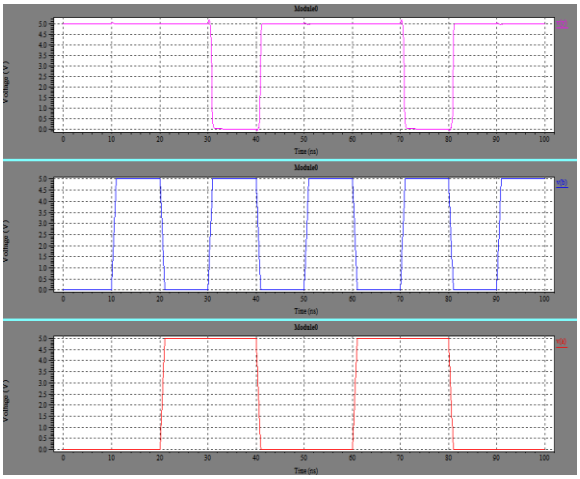

Fig.7.3.1.NAND gate simulation output

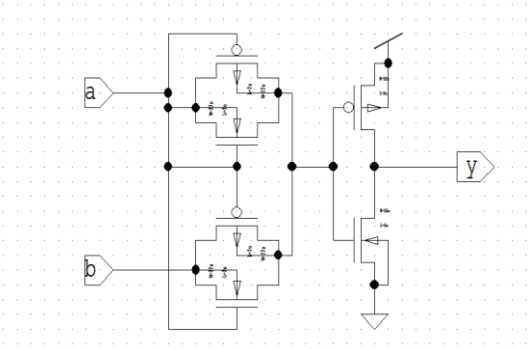

Fig.7.4.NOR gate circuit using TG

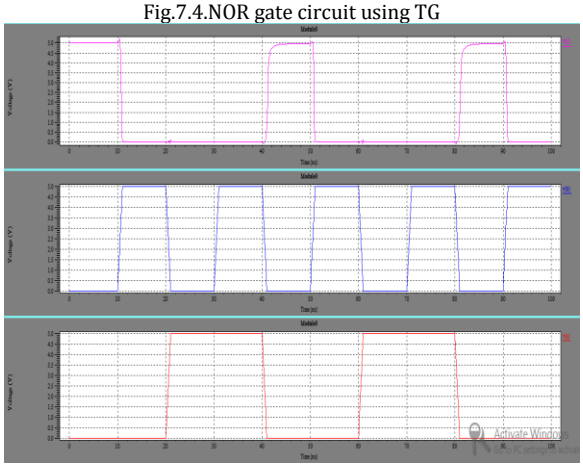

Fig.7.4.1.NOR gate simulation output

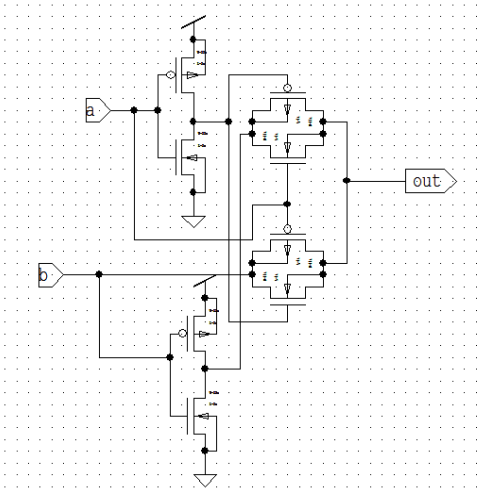

Fig.7.5.XOR gate circuit using TG

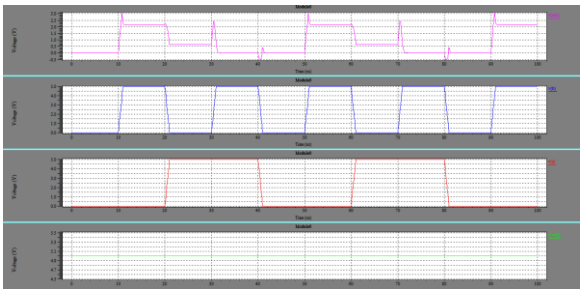

Fig.7.5.1.XOR gate simulation output

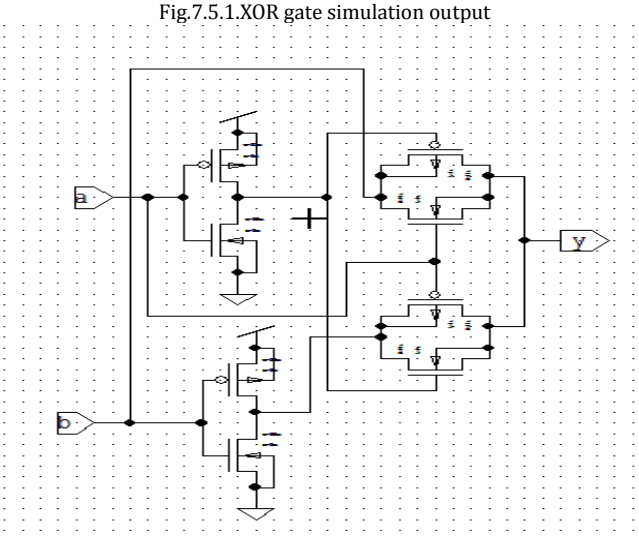

Fig.7.6.XNOR gate circuit using TG

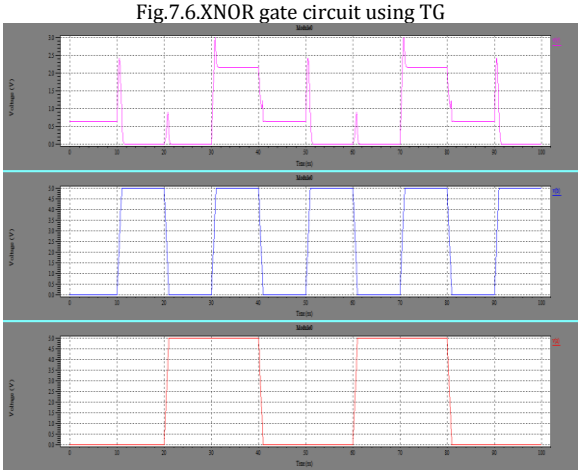

Fig.7.6.1.XNOR gate simulation outputs

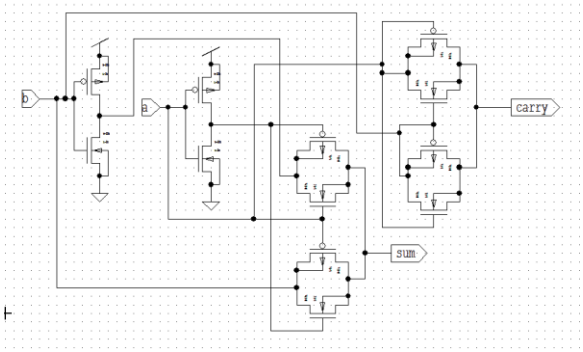

Fig.7.7.Half adder circuit using TG

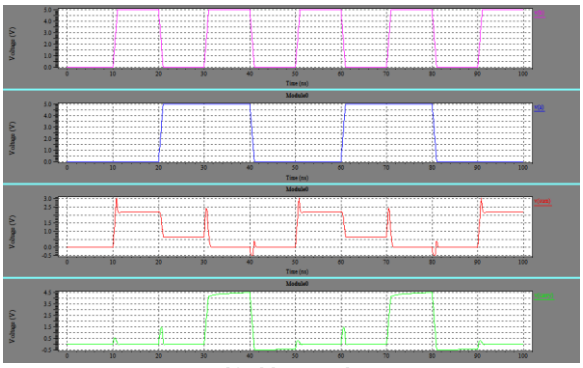

Fig.7.7.1.Half adder simulation output

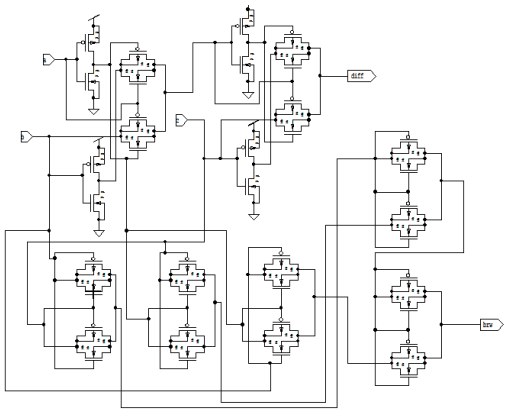

Fig.7.8.Full subtracter circuit using TG

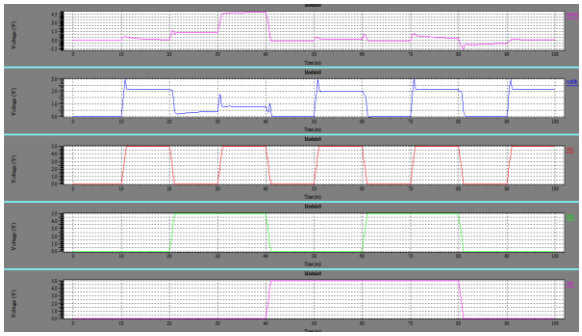

Fig.7.8.1.Full subtracter simulation output

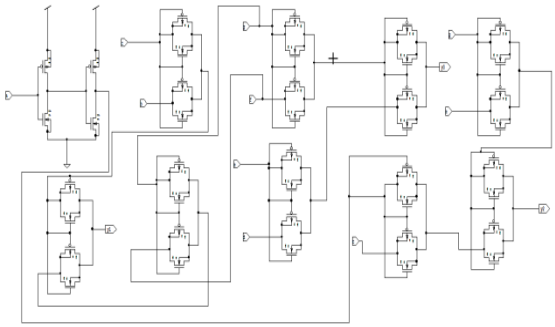

Fig.7.9.8:3Encoder circuit using TG

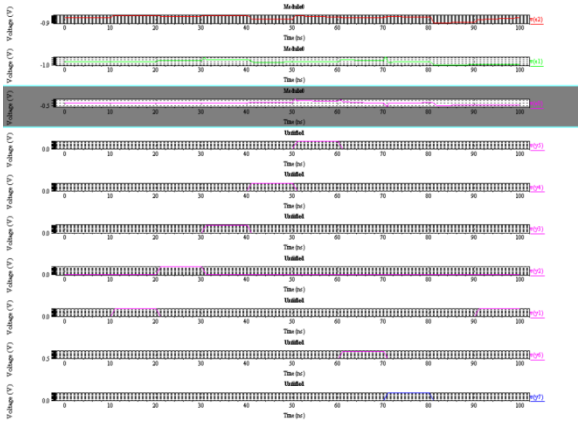

Fig.7.9.1.8:3Encoder simulation output

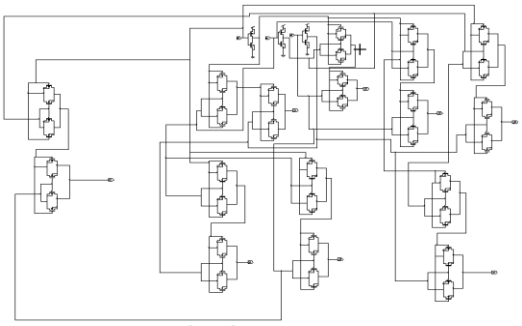

Fig.7.10.3:8 decoder circuit using TG

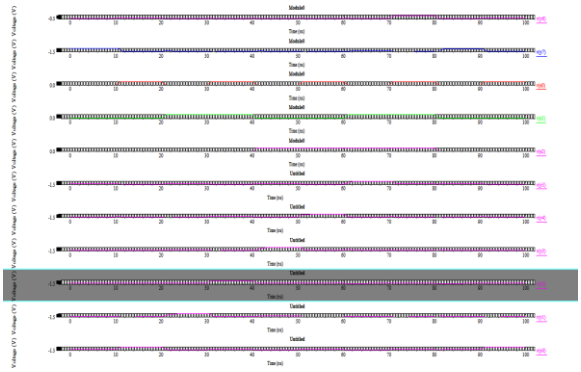

Fig.7.10.1.3:8 decoder circuit simulation output

VIIICONCLUSION

Software used for simulating the combinational circuits using Transmission Gate is TANNER.All circuits are designed in 125nm technology. This paper is designed to optimize power and leakage current by using transmission gate logic(TGL).

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Table I - Result analysis of combinational circuits

S.No	Name of the Circuit	Average Power (watts)	Max Power (watts)	Time for Max Power (µs)	Min Power (watts)	Time for Min Power (µs)
1	OR GATE	$416.6134*10^{-2}$	$139.9997*10^{-4}$	0.040	$833.1245*10^{-9}$	0
2	AND GATE	$417.0558*10^{-2}$	$163.1133*10^{-4}$	0.080	$833.1245*10^{-9}$	0
3	EX-OR GATE	$624.9878*10^{-2}$	$176.3541*10^{-4}$	0.040	$290.9474*10^{-12}$	0.070
4	EX-NOR	$520.334*10^{2}$	$200.2721*10^{-4}$	0.081	$245.4371*10^{-12}$	0.030
5	NAND	$207.8581*10^{-2}$	$642.7982*10^{-5}$	0.080	$995.2805*10^{-12}$	0.041
6	NOR	$207.0932*10^{-2}$	$434.6253*10^{-5}$	0.041	$110.1599*10^{-11}$	0.040
7	HALF ADDER	$624.9878*10^{-2}$	$171.5810*10^{-4}$	0.080	$291.0272*10^{-12}$	0.071
8	FULL ADDER	$178.872*10^{3}$	$574.2268*10^{-4}$	0.081	$566.7315*10^{-12}$	0.071
9	HALF SUBTRACTOR	$833.2721*10^{-2}$	$200.642*10^{-4}$	0.041	$284.5021*10^{-12}$	0.030
10	FULL SUBTRACTOR	$166.6554*10^{-1}$	$297.1029*10^{-4}$	0.081	$612.2090*10^{-10}$	0.063
11	MULTIPLEXER	$124.9131*10^{-1}$	$206.2913*10^{-4}$	0.081	$297.6934*10^{-12}$	0.060
12	DE-MULTIPLEXER	$833.0997*10^{-2}$	$210.2580*10^{-4}$	0.081	$246.3841*10^{-12}$	0.030
13	ENCODER	$208.4288*10^{-2}$	$143.253*10^{-4}$	0.080	$240.9345*10^{-10}$	0.042
14	DECODER	$228.9880*10^{-1}$	$330.631*10^{-4}$	0.081	$393.6401*10^{-12}$	0.071