A survey on effective Automatic Test Pattern Generator for self-checking Scan - BIST VLSI circuits

G. Naveen Balaji[1], S. Chenthur Pandian[2], D. Rajesh[3]

[1]*Assistant Professor, Department of ECE,*
SNS College of Technology, Coimbatore, India
yoursgnb@gmail.com, Researcher Id- B-9448-2016
[2]*Principal,*
SNS College of Technology, Coimbatore, India
principal@snsct.org
[3]*UG Student, Department of ECE,*
SNS College of Technology, Coimbatore, India
rockzoft23@gmail.com, www.rajeshd.in, Researcher Id- C-1968-2016

---***---

Abstract -*This paper attempts to show the survey on ISCAS89 Sequential Benchmark circuits. Gate delay, propagation delay, no. of flip flops and total number of gates are listed and compared for benchmark circuits.The circuits were built in .asl file and simulated using AUSIM L2.3.Operating temperature, marginal supply voltage as well as an increased output load capacitance leads to variation in gate delay or in propagation delay.Depending on the circuit components placed one after another, the delay varies. All aspectsare compared for the Benchmark circuitsfrom s27 to s38584.*

***Key Words*: Linear assembly, Test Pattern Generator, Linear Feedback Shift Register, Weighted and Transition Density Pattern**

1.INTRODUCTION

The analysis of number of flip flops and total number of gates, gate delay and propagation delay for the benchmark circuits. The combinational connection ofinvertors, AND, NAND, OR, NOR in the benchmark circuits are compared. Comparison of all ISCAS89 benchmark circuits has least gate delay and propagation delay are 6 and 22, maximum of 127 and 1636 respectively.

2. DESIGN FOR TESTABILITY (DFT)

Design for testability is an IC design technique and adds testability feature for scheming hardware product. The added topographies make easier to develop and built-up tests to the proposed hardware.The purpose of built-up tests is to validate no manufacturingdefects for the product and that could undesirably affect the product’s correct performance.The tests are generally propelled by impulsive test equipment that execute test programs.

3. SCAN-BIST

Scan chain is a method used in design for testing. The aim of the chain is to make testing easier by providing a simple way to set and observe every flip-flop in an Integrated Circuit. The basic structure of scan includes the following set of signals in order to control and observe the scan mechanism.

Scan-output and scan-in define the output and input of a scan chain. Each input drives only one chain and scan out observes one as well in a full scan mode. A scan enable pin is a special signal that is added to a design. When this signal is stressed, every flip-flop is connectedinto a long shift register.

During shift phase and the capture phase the clock signals are used guiding all flip flops in the chain. An arbitrary pattern can be inserted into the chain of flip-flops, and everystate ofthe flip-flop can be observed. In a full scan design, automatic test pattern generation (ATPG) is particularly simple.

Even a simple stuck-at fault requires a order of vectors for recognition in a sequential circuit. Also, due to the presence of memory elements, the controllability and observability of the internal signals in a sequential circuit.In general much more problematic than those in a combinational logic circuit. These aspects make the difficulty of sequential ATPG much higher than that of combinational ATPG.

4. BENCHMARK CIRCUITS

It is primarily for testing. A benchmark is a point of reference by which something can be restrained. In surveying, a "bench mark"is apermanent mark established at a known elevation that is used as the basis for measuring the elevation of other topographical points. It is widely available, modern design to spur research on DFT.

5.PROPAGATION DELAY

When the input to a logic gate becomes stable and valid to change, to the time required for the output of that logic gate is stable and legal to change. Often on manufacturers' datasheets this mentions to the time required for the output to stretch 50% of its final output level when the input variations to 50% of its final input level. To process data at a faster rate and improving overall performance by reducing gate delays in digital circuits that allows them. The determination of the propagation delay of a combined circuit requires todetecting the longest track of propagation delays from input to output and by adding each tpd time along this track.

The difference in propagation delays of logic elements is the major contributor to glitches in asynchronous circuits as a result of race conditions.The principle of logical effort utilizes propagation delays to compare designs implementing the same logical statement.

Operating temperature, marginal voltagesupply as well as an increased output load capacitance leads to increase in Propagation delay. Propagation delay can be increased by the latter is the largest contributor. If the output of a logic gate is connected to a long trace or used to drive many other gates the propagation delay increases substantially.

Wires have an estimated propagation delay of 1 ns for every 6 inches (15 cm) of length. Logic gates can have propagation delays ranging from more than 10 ns down to the picosecond range.

It is a time related with any digital circuit and is the time between when an input to the circuit varies until that variation propagates through the circuit and changes the output. Every digital gate (And, Or, Inverter...) has its own propagation delay. For single gates this delay can be very short, maybe somewhere around nanoseconds or shorter. If the circuit grows larger and more components are placed one after another, the delay increases too.

6. GATE DELAY

The input of the logic gate changes its state to 0's or 1's. The output of the gate will probable to change its state as its result. The output will not change rapidly when the input changes. Instead, the output will change after a small delay. This delay is called gate delay. Ideally, this delay is a small as possible; typically, it is on the order of few nanoseconds or less. Often the delay, when the output changes from low or high is a different value than the delay when the output changes from high to low.It isnon-zero-time amount of time to charge or discharge a capacitor in which the voltage cannot be changed instantaneously.

7.FAN-IN

After the minimization of circuit level and mapping to the primary gates (AND or OR) with infinite fan-in and fan-out. Minimum circuit Depth is 2 for all logic circuits in accordance to this definition. Because any logic functions can be expressed in sum of product form without any fan-in that limits all the product expressions can be executed by AND gates and summed by one OR gate.

The acute path includes in one AND gate and one OR gate, corresponds to circuit depth of 2. The assumption of infinite fan-in and fan-out are invalided. The dependence of the circuit is based on both gate fan-in and fan-out maximums.

When the maximum fan-in is 4 the the depth will be 2. When the maximum fan-in is decreased by 2, then the depth of the circuit will be increased by 4. The simulation results allow us to statistically qualify the tendency of the circuit depth versus limitation of fan-in for the multiple input and multiple output of the combinational logic circuits.

8. FAN-OUT

The current from the output is sufficient to charge the load gate(s') input capacitor(s') and wire capacitor within time. For OE circuits the maximum fan-out is limited by the ratio of the gate's output. After minimizing the circuit might require large fan-out that is beyond the maximum fan-out limits to the existing gate.

Both methods cause circuits to increase in depth. To evaluate the circuit depth increase caused by limiting fan-out. A large gate fan-out is significant in succeeding a smaller circuit depth.

9. LOGIC GATES

A logic gate is a fundamental building block of a digital circuit. Most logic gates have two inputs and one output. Every terminal is in one of the two binary conditions low (0) or high (1), represented by unlike voltage levels. The logic state of a terminal can, and generally does, change often, as the circuit processes data. In most logic gates, the low state is about zero volts (0 V), while the high state is approximately five volts positive (+5 V).

10. TEST OPTIMIZATION TECHNIQUE

Test optimization will make a build potentially comprehensive a lot faster than a full build and test run. It should do this without substantially compromising the property of the feedback it gives; in other words, a quicker pass or fail result, but a reasonably precise pass or fail. There are two ways of ensuring a build completes quickly:

1. Run only the tests required to confirm the validity of the changes that triggered the build.
2. Run all the tests but in an optimal order: any failed tests from the previous build, all tests covering modified code, then in ascending order by test invocation time.

S.No	Circuit	DFF	Inverters	AND	NAND	OR	NOR	Total Gates	GD	PD
1	s27	3	2	1	1	2	4	10	6	22
2	s208	8	38	21	15	14	16	104	11	40
3	s298	14	44	31	9	16	19	119	9	49
4	s344	15	59	44	18	9	30	160	20	69
5	s349	15	57	44	19	10	31	161	20	69
6	s382	21	59	11	30	24	34	158	9	51
7	s386	6	41	83	0	35	0	159	11	62
8	s400	21	56	11	36	25	34	162	9	52
9	s420	16	78	49	29	28	34	218	13	54
10	s444	21	62	13	58	14	34	181	11	58
11	s499	22	32	0	60	40	20	152	12	56
12	s510	6	32	34	61	29	55	211	12	58
13	s526n	21	54	55	22	28	35	194	9	50
14	s635	32	128	31	34	63	30	286	127	375
15	s641	19	272	90	4	13	0	379	74	223
16	s731	19	254	94	28	17	0	393	74	243
17	s820	5	33	76	54	60	66	289	10	118
18	s832	5	25	78	54	64	66	287	10	121
19	s838	32	158	105	57	56	70	446	17	89
20	s938	32	158	105	57	56	70	446	17	89
21	s953	29	84	49	114	36	112	395	16	69
22	s967	29	99	49	102	37	107	394	14	71
23	s991	19	220	47	101	118	33	519	59	289
24	s1196	18	141	118	119	101	50	529	24	106
25	s1238	18	80	134	125	112	57	508	22	112
26	s1269	37	132	235	74	41	87	569	35	147
27	s1423	74	167	197	64	137	92	657	59	282
28	s1488	6	103	350	0	200	0	653	17	148
29	s1494	6	89	354	0	204	0	647	17	149
30	s1512	57	367	98	92	176	47	780	30	163
31	s3271	116	537	372	224	159	280	1572	28	116
32	s3330	132	974	577	17	219	2	1789	29	132
33	s3384	183	615	704	0	317	49	1685	19	73
34	s4863	104	742	1175	0	425	0	2342	---	---
35	s5378	179	1775	0	0	239	765	2779	25	179
36	s6669	239	1009	1476	0	595	0	3080	---	---
37	s9234	228	3570	955	528	431	113	5597	58	228
38	s13207	669	5378	1114	849	512	98	7951	59	669
39	s15850	597	6324	1619	968	710	151	9772	---	---
40	s35932	1728	3861	4032	7020	1152	0	16065	---	---
41	s38417	1636	13470	4154	2050	226	2279	22179	47	1636
42	s38584	1452	7805	5516	2126	2621	1185	19253	56	1452

CONCLUSION

According to the analysis the circuit has different gate delay and propagation delay. The gate delay affects the circuits by delay time effect of gates to produce the fanout of gates. The propagation delays emerge as the important time constraints for producing the output.

REFERENCES

1. Reeb, Birgit, and Hans-Joachim Wunderlich. "Deterministic pattern generation for weighted random pattern testing." Proceedings of the 1996 European conference on Design and Test. IEEE Computer Society, 1996.

2. Balaji, G. Naveen, and S. Vinoth Vijay. "Arbitrary Density Pattern (ADP) Based Reduction of Testing Time in Scan-BIST VLSI Circuits." International Journal of Science, Engineering and Technology Research 2, no. 6 (2013): pp-1237.

3. Pattunarajam, P., and G. Naveen Balaji. "ECONOMICAL SCAN-BIST VLSI CIRCUITS BASED ON REDUCING TESTING TIME BY MEANS OF ADP." International Journal of Science, Engineering and Technology Research 2.5 (2013): pp-1088.

4. Wang, Seongmoon, and Sandeep K. Gupta. "DSLFSR: a BIST TPG for low switchingactivity." Computer-Aided Design of IntegratedCircuits and Systems, IEEE Transactions on 21.7(2002): 842-851

5. Wang, Yi, and Gui-Juan Xu. "Research on a lowpower test generator about integratedcircuits." Information and Computing Science(ICIC), 2012 Fifth International Conference on.IEEE, 2012.
6. Noor, NurQamarinaMohd, AzilahSaparon, andYusrinaYusof. "An overview of microcode-basedand FSM-based programmable memory built-inself test (MBIST) controller for coupling faultdetection." Industrial Electronics & Applications,2009. ISIEA 2009. IEEE Symposium on. Vol. 1.IEEE, 2009.

7. Mosin, Sergey G., Natalia V. Chebykina, and MariaS. Serina. "Technique of LFSR based test generatorsynthesis for deterministic and pseudorandomtesting." CAD Systems in Microelectronics(CADSM), 2011 11th International ConferenceThe Experience of Designing and Application of.IEEE, 2011.