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"A Power Analysis of SRAM Cell Using 12T Topology for Faster Data Transmission: A Review"

Priya Thakare[1], Sanjay Tembhurne[2]

[1] *M.Tech. Scholar, Department of Electronic & Communication, G.H.R.A.E.T, Nagpur,India, priyathakare555.pt@gmail.com*
[2] *Asst. Professor, Department of Electronic & Communication, G.H.R.A.E.T, Nagpur, India, sanjay.tembhurne@raisoni.net*

Abstract - *Nowadays circuit designers are facing a major problem of chip high power consumption. This paper represents improved 12T SRAM cell with reduced leakage current and improved performance on 180 nm technology. The SRAM cell is the demand of high speed digital computing system. The switching of transistor decides the power consumption in any digital cell. Leakage current during off state of device is responsible for power consumption in memory cell. To compare the proposed work with existing structure available with 12T. The proposed design reduces the power consumption and increases the speed of data transmission.*

Key Words: *SRAM Cell , CMOS , leakage current , power , 12T SRAM Cell , read , write*

1.INTRODUCTION

The SRAM cell is the main memory device used in modern digital system. Memory refers to the computer hardware device use to store information. Memories are of two types. Static random access memory (SRAM) and dynamic random access memory (DRAM).

A)SRAM : SRAM is a semiconductor memory use to store each bit, it is a volatile memory. It depends upon the constant voltage supply to hold the stored data. Non volatile random access memory is similar in operation as that of volatile memory. But they save the data when power supply is lost. SRAM does not require a constant refresh cycle. Figure 1 shows the diagram of SRAM.

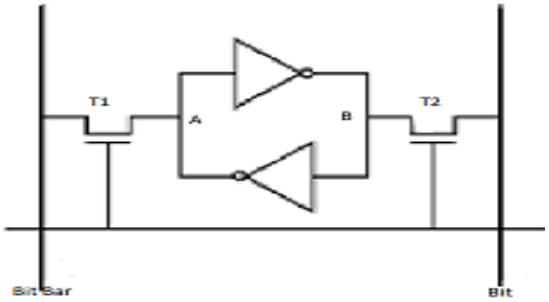

Fig-1: SRAM Cell

B)DRAM : Dynamic random access memory cell require a capacitor to store the data. DRAM require as compare to SRAM. It requires a constant refresh cycle at all time. So that it consumes more power as compare to SRAM cell. Figure 2 shows the diagram of DRAM.

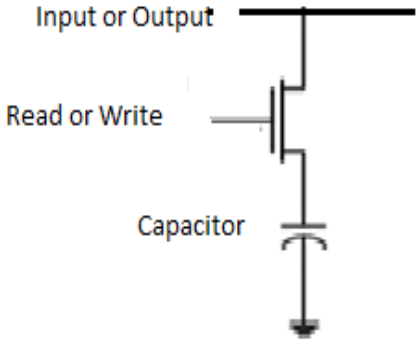

Fig-2 : DRAM Cell

SRAM cell is faster cell but it has large leakage current. So it is necessary to design a SRAM with low leakage current and power consumption. There are many ways to reduce power consumption such as reducing power supply, using stack effect and clock gating technique. So that first is necessary to reduce the threshold voltage to maintain high drive current and performance of cell. For the reduction of power dissipation and increase the performance we analyze the 12T SRAM cell.

1.1 4T SRAM Cell

SRAM cell is designed to have proper read operation and reliable write operation. The structure of 4T SRAM cell is as shown in figure 3.

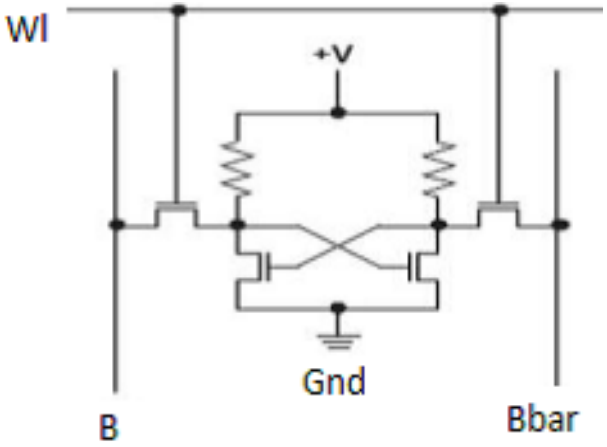

Fig-3: 4T SRAM Cell

A typical SRAM uses two p-MOS , two n-MOS and load resistor. The load resistor are made up of poly silicon or depletion type of n-MOS or p-MOS. SRAM operated in three modes:

A)Stand By mode : In this mode, word line is not asserted. So that the pass transistor are deactivate. So that no read and write operation is performed in this mode and ram hold the stored data. The power require to hold the data is more.

B)Read mode : Read operation is performed by first enabling the word line and the pass transistor are activated. The voltage at bit line(B) is kept high and the bit bar line(Bbar) is pulled to low. The difference between two voltages is detected high, so 1 is read. When the difference between them is minimum , it means 0 is read through cell.

C)Write mode : When 1 has to write in to the cell that time it is necessary to make bit line high and bit bar line at low voltage. Similarly when 0 has to write in to the cell then bit line(B) is kept at low whereas bit line bar(Bbar) is at high voltage.

1.2 6T SRAM Cell

6T SRAM cell is symmetrical in nature. The circuit of 6T is as shown in figure 4.

In this circuit, two p-MOS and four n-MOS are used. The bit line(B) is connected to transistor N2 and bit line bar (Bbar)is connected to transistor N1. Bit line and bit line bar is used to data to be written in to the cell. And word line is use for read and write operation. Q and Qbar are the storing nodes. When node Q stores 0 , the node Qbar stores 1. In this case transistor N4 and P2 are turned on. Also P1 and N4 turned off.

When word line is not selected at that time pass transistor N1 and N2 are turned off and circuit is on idle mode(hold mode). When data is to write in the cell, first data has to apply to the bit line(B). Bit line bar(Bbar) has compliment of bit line data. When data 1 is to written on cell , first select the word line (WL=1) so that the transistor N1 and N2 are enabled, and bit line is also 1 and data is stored in to the cross coupled inverter. When data 0 has to written in the node storing 1, the corresponding bit line is applied with voltage 0 and bit line bar to Vdd and also word line (WL) to vdd .

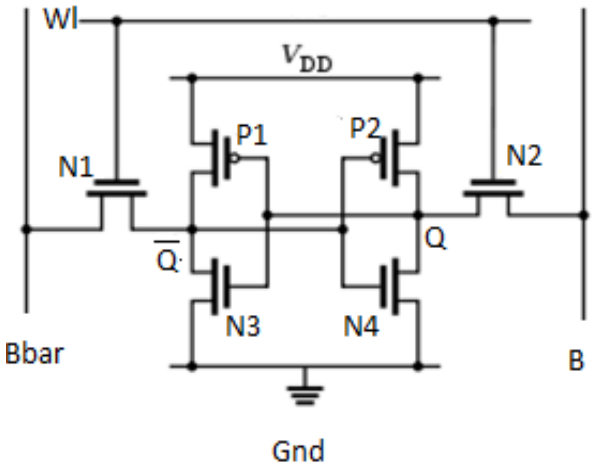

Fig-4: 6T SRAM Cell

During read operation, pre-charged the bit line and bit line bar to high and turn on word line (WL). The transistor N1 and N2 are turn on. Values stored in Q and Qbar are send to bit line. Bit line and bit line bar will be pulled down depending on Q and Q. If Q=0 , Qbar=1 , Bit line (B) discharges and bit line bar (Bbar) stays high and vice versa.

2. LITERATURE REVIEW

Jaydeep P. Kulkarni [1] , gives the ultra voltage operation of different SRAM cell. By lowering the supply voltage ,the ultra voltage operation is performed. The proposed ST-2 bit cell gives 1.6 times higher read static margin and 2 times write static margin as compare to 6T SRAM. In this paper 6T/8T/10T/ST SRAM topologies are evaluated for achieving low voltage operation. Result are evaluated at 130nm technology, which clearly give the effectiveness of proposed bit cell for successive ultra low voltage operation.

Ambrish Mall, Suryabhan Pratap Singh, Manish Mishra, Geetika Shrivastava[2], this paper gives the brief development in low power circuit. The power consumption is more in stand by mode. The proposed circuit contains a series connected tail transistor which turn down the leakage current because of this , cell achieves low power consumption. The proposed 12T SRAAM cell is compare with low power 10T SRAM cell on 45nm and 32nm technology, it gives the power reduced by 45.94% (0.4v) and 31.08% (0.3v) res.

Mohsen Imani, Haleh Alimohamadi[3] Proposed low power and reliable 12T SRAM cell with with 16nm at 800mv

supply voltage cmos technology . The proposed 12T SRAM cell is comare with the 9T and 10T SRAM cell. The leakage current is reduces by using by using two stack transistor at read path. The reliability of cell is also increases by increasing read SNM. The proposed cell has 5.5% and 27.4% higher rwead SNM from 9T and 10T res. The power consumption of proposed cell has 35.5% and 43.8% lowered as comparison of 9T cell and 10T cell.

K.G.Dharani[4] , this paper gives the comparative analysis of 6T, 8T and 12T SRAM memories by power , layout and current values . during read and write operation current values decreases or remain same in 6T , 8T, 12T but the power consumption is increases in 12T. But 12 T has a high capability to hold the data . This paper specifies that 6T has very less read margin with 8T transistor . But 8T has high write noise margine.

Mekala Tajeswar, P. Brundavani[5] ,in this paper, the working of 12T SRAM cell on multi threshold CMOS technology are evaluated. This paper gives the reduction in power consumption of SRAM cell by adding transmission gate. The leakage current during hold mode is reduced by applying two sleep transistor and swing voltage is reduced by applying two voltages at the output. On the basis of power consumption, the proposed 12T SRAM cell is compared with the 6T SRAM cell. The result analyzed as the power dissipation in 6T SRAM is 0.182mw and power dissipation at 12T SRAM is 0.169mw. Proposed 12T SRAM gives the better performance and high speed data transmission with or without recovery boosting technique.

M.Gangasukanya, P.Asiya Thapaswin[6], this paper introduced a 12T SRAM with a low power consumption and high data transmission speed at 45nm technology. The proposed 12T SRAM cell is studied at different temperature. The proposed SRAM cell has a low Voltage transistor and two high voltage sleep transistor to minimize the power consumption during changing of mode from hold to active state. So that the static power is also reduced in the cell. The dynamic power id reduced in this paper by applying two voltages at the output. The first voltage is applied to the bit line and second one is applied to the bit line bar , which overcome the swing voltage. So that the reduction in swing voltage there in reduction in leakage current also during hold mode. By this technique the power consumption of SRAM cell is reduced in this paper.

P.Pavan Kumar, Dr. R Ramana Reddy, M.Lakshmi Prasanna Rani[7],this paper gives the 4T SRAM with low power consumption with reliability of SRAM. The proposed 4T SRAM is compared with the 6T SRAM and basic structure of 4T SRAM. The software used for this simulation was mentor graphics at 130nm technology. The nmos and inverter were used to design the proposed 4T SRAM. In this paper static power is reduced by 41% , total power is reduced by 32% , delay is reduced by 36% and occupies 32.46% less area as compare to conventional 4T SRAM cell.

3. PROPOSED WORK

Power analysis technique use is taken from the paper presented by Jaydeep P. Kulkarni [1] and Ambrish Mall, Suryabhan Pratap Singh, Manish Mishra, Geetika Shrivastava[2] as mentioned above. Based on those results we will design the 12T SRAM in CMOS technology. The Proposed 12T SRAM circuit will have low power and delay will be reduced. The power consumption of cell is mainly the static or dynamic power. The dynamic power will depend on the time taken by the input signal to change the state from low level to another level. Static power is mainly during off state or when leakage current flow through the device. To overcome the above problem some average merits needed to bring the current flowing through device to zero or bypass the leakage current from off device. As the delay reduces, power will also be reduced. The proposed SRAM will be used in high speed application devices. Low power consumption can be achieved by reducing a number of devices in design such as ; by reducing static power, which is mainly due to impurity/ carrier present in the device which gives the result in the form of leakage current mainly responsible for static power losses. In this paper the proposed idea will concentrate on reducing the number of MOS devices used by previous designer. The design layout of the simulation will be carried on the tanner tools 0.18um CMOS technology. As the number of transistor increases the storing capacity of SRAM is increases as well as the power consumption of cell is also increases. The main objectives of the proposed SRAM cell are to reduce the power consumption and improves the speed of data transmission by reducing the delay. The goal can be achieve by

4. EXPECTED OUTPUT

These days, in a electronic devices having very high demand for low power consumption devices. This paper introduced a 12T SRAM with low power consumption with a faster data transmission speed. Power consumption of 12T SRAM cell is higher as compare to 4T/6T, because the number of transistor increases but the capacity of holding the data is higher in 12T SRAM cell

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