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# LVPLL with MCSS Charge Pump in 90nm CMOS for SoCs

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**Abstract -** *A Low voltage Power Efficient Phase Locked Loop is designed for SoCs. A MCSS Charge Pump is introduced to reduce leakage current and current mismatch. In order to achieve wide tuning range at low VCO gain Kvco. A Low voltage VCO (LV-VCO) for low voltage application is designed by a Ring Oscillator using 4-stage differential delay cells with low voltage segmented current mirror (LV-SCM) for biasing purpose. Proposed PLL is implemented in 90nm CMOS Technology and measures phase noise and power consumption for enhanced CP and RO-VCO.*

***Key Words***: SoC, Charge Sharing, Charge Pump, TSPC, Ring Oscillator, Microwind

## 1. INTRODUCTION

Today, success of electronic market depends on highest level of system integration in order to achieve low power and low cost without compromising speed or performance for mass production in the consumer, wireless and computer market. System-on-Chip (SoC) allows to integrate analog as well as digital circuits on a single chip in order to achieve analog mixed signal devices such as ADC, PLL, and DAC etc. In nanoscale CMOS technologies, due to feature size reduction it is necessary to scale down supply voltage to achieve reliable operation of transistors. Phase locked loop (PLL) is one of the most widely used mixed signal device used for various applications such as on-chip clock generations in various applications such as frequency synthesizers, frequency tracker and clock recovery circuits. But PLL is one the most power consuming device and each and every block should be optimized in order to minimize overall power consumption and to make design power efficient.

### 1.1 PHASE LOCKED LOOP

*Phase Locked Loop* is basically a closed loop frequency control system. PLL Clocks are used when the system needs to minimize the propagation delay. It is able to do this by acting as a phase detector to keep an input clock in phase with an output frequency of VCO which is fed back to phase detector through feedback network. As the Fig-1 suggests, Functional building blocks of PLL are as follows:

1) Phase Frequency Detector
2) Loop Filter
3) VCO

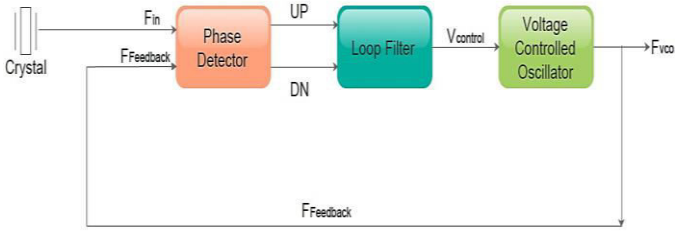


**Fig -1**: Block Diagram of Traditional PLL

Phase Frequency Detector compares the Feedback frequency from VCO and input reference frequency and generates a DC level which is proportional to Δϕ (i.e. Phase Difference of input and output) [1]. Low Pass Filter as the name suggests filter out high frequency components and allow DC components to achieve pure DC $V_{control}$. It is an oscillator which is controlled by a DC voltage and generate output frequency based on it. Though this type of PLL is comprised of mostly analog blocks and it is difficult to design analog circuits in deep submicron CMOS technology at low supply voltage. As a result poorly performed PLL can be a bottleneck in the current and coming computational systems.

### 1.2 ADVANCES IN PLL

In SoCs, there are multiple functional blocks which require different clock frequencies thus clock generators with wide tuning-range are essential. In low voltage applications, wide frequency range may cause a large VCO gain which can increase VCO sensitivity towards power/ground noises. Earlier, LC-VCOs were used to achieve smaller output jitter and good phase noise performance with low power consumption. However, the tuning-range of LC-VCO (around 10-20%) is relatively less compared to RO-VCO (>50%) [5]. As a result output frequency may fall out of desired range due to process variations.

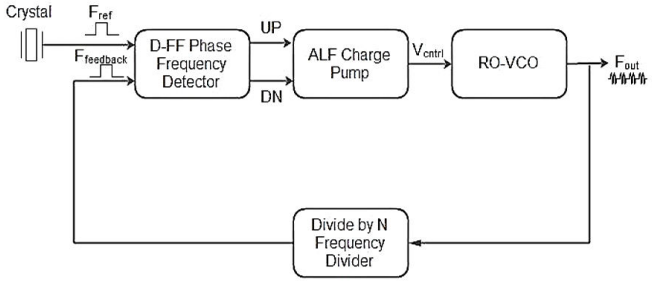


**Fig -2**: Block Diagram of Modified PLL

Also phase noise performance of PLL depends on quality factor of inductor and it is difficult to achieve required quality factor in digital CMOS technology. As Spiral inductor in LC-VCO occupies a large amount of chip area which reduces advances to be achieved by scaling [6].
At low supply voltages large threshold voltages of transistors may cause CMOS switching to slow down which can prevent VCO and frequency divider to operate on high frequencies. There are several methods developed to design a low voltage analog circuit design: (1) special low- VT devices [10], (2) on-chip clock and gate voltage boosting [11] and (3) body-biasing and body-driven circuits [12] [13]. Low-VT devices requires extra masks during fabrication and incurs higher production costs. On-chip voltage boosting introduces long-term reliability concerns, especially for nanoscale CMOS devices. Body-biasing and body-driven circuits cause latch-up problems. To avoid forward biasing of the body–source junction, the PMOS body (NMOS) connects to the VDD (GND) [13].

A 90-350 MHz LVPLL has been proposed using 0.5V supply voltage. Section 2 shows architecture of proposed PLL. Conclusions are drawn in Section 3.

## 2. ARCHITECTURE OF PROPOSED LVPLL

Architecture of proposed LVPLL is shown in Fig-3. Here, the MCSS charge pump (CP) circuit operates at low supply voltage in order to achieve higher supply voltages to drive analog circuit blocks and its small parasitic capacitance helps to decrease switching time of PMOS and NMOS resulting in reduction in leakage current. The Low voltage VCO is a Ring oscillator (RO) which consists of 4-stage delay cells and a low voltage segmented current mirror (LV-SCM) for biasing. To operate over wide frequency range, low $K_{VCO}$ is essential thus LV-SCM is added with LV-VCO to achieve a low $K_{VCO}$ and multi-band frequency output. Frequency Divider is used to enhance operating speed of LVPLL.

### 2.1 MCSS CHARGE PUMP

Various Charge Pump Architectures have been reported serving different purposes to different targeted applications [2]. Single Ended CPs are popular in SoCs as they do not require any additional loop filters and consume low power operating at low supply voltage. In the previous work, switches at the drain of the current mirror causes charge injection in DC control voltage of VCO $V_{cntrl}$ which make PLL not to remain in locked condition as VCO is not able to maintain a minimum constant phase difference between its output frequency and input frequency [14].
Furthermore, there is a charge sharing problem between loop filter capacitor and MOS parasitic capacitance. The cascade switches in Single ended Charge Pump requires voltage headroom for given supply voltages $V_{DD} > V_{DSP}+V_{DSN}+V_{DSATP}+V_{DSATN}$ where $V_{DSP}$, $V_{DSN}$ are drain to source voltages of PMOS and NMOS respectively and $V_{DSATP}$, $V_{DSATN}$ are drain source saturation voltages of PMOS and NMOS respectively. Thus, these previous designs of Charge pump

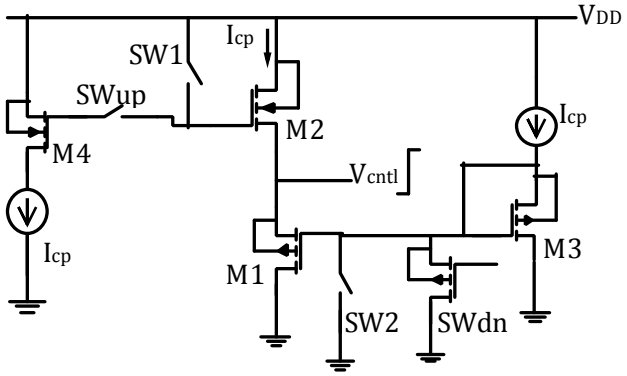


**Fig -3**: Schematic of MSCC Charge Pump

are facing current mismatch during switching activities and charge sharing in VCO control voltages thus these designs are not suitable for low voltage operations [7].
A Modified Charge Sharing Scheme (MCSS) is proposed here. In this scheme, CP switches control gate instead of drain or source which creates a current path from power to ground and dc leakage current IL of M1 transistor causes a voltage drop down in $V_{cntrl}$. This leakage current can be reduced by inserting two switches SWUP and SWDN to control UP and DN signals respectively. As shown in Fig-3, when UP=0.5 and DN=0 SW2 and SWUP are turned on and SW1 and SWDN are turned off. With this arrangement current path is cut off and it will minimize leakage current. In addition, M3 an M4 are remains in saturation region thus circuit produces less noise and higher operational switching activities compared to conventional CP.

### 2.2 LV-VCO

VCO is an important component of PLL and it plays an important role to achieve wide tuning-range at low supply voltage and to achieve a power efficient system. Conventional ring VCOs have some advantages to offer [5]. To obtain high output frequency, LC-VCO is a good choice as it provides high noise rejection capability but it occupies large area than ring oscillator on chip and faces difficulty to produce multi-phase output frequency [3]. In the proposed LV-VCO, 4 stage differential ring oscillator is chosen to reduce supply noise and to produce 8-phase output frequency. Fig-4 shows LV-VCO consist of 4-stage delay cells and LV-SCM. LV-SCM converts digital code into analog current so delay cells can produce multi band output frequencies. For low voltage applications, cascaded design of delay cell must be avoided in order to prevent supply noise in output frequency [4]. Drain current of PMOS transistor is:

$$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W_p}{L_p}(V_{SG} - |V_{TP}|)^2(1 + \lambda_p V_{SD}) \quad \text{... (1)}$$

The delay cells of LV-VCO consists of a pair of differential input NMOS and a pair of PMOS load. Current through PMOS load can be adjusted by tuning the $V_{cntrl}$ which gives a small KVCO compared to conventional PMOS loads which leads to a wider range of output frequency compared and produces multi-phase signals.

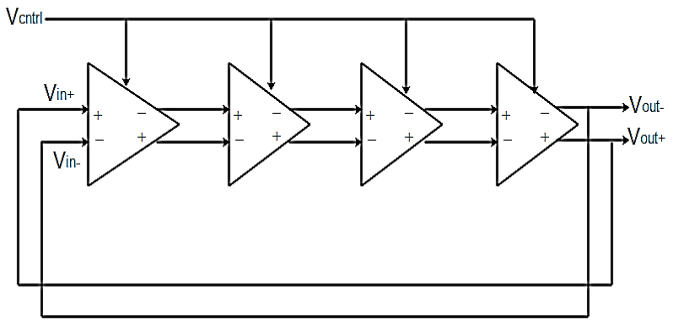


**Fig -4:** 4-stage Delay Cells in RO

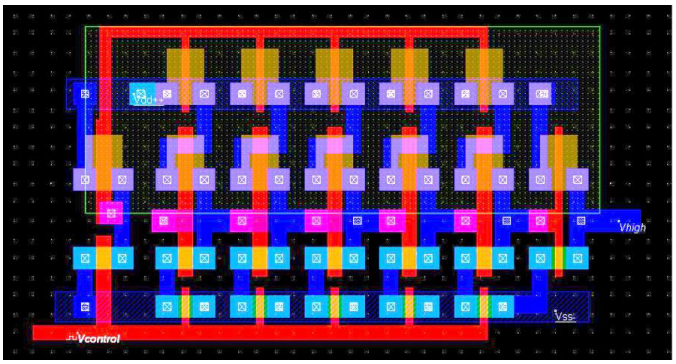


**Fig -5:** Layout of LV-Ring VCO in Microwind

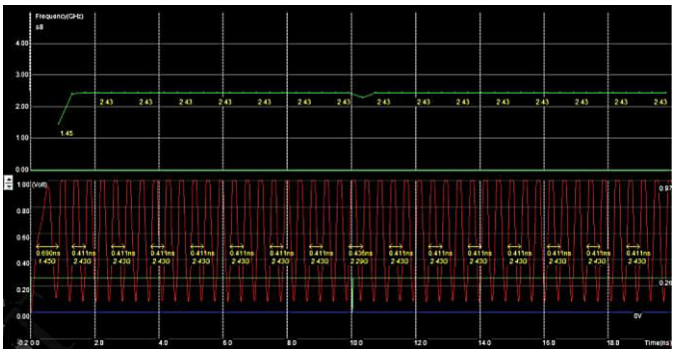

**Fig -6:** Simulation of LV-Ring VCO in Microwind

## 2.3 FREQUENCY DIVIDER

Frequency Divider is an essential building block of PLL. As the output frequency of VCO might turn out in MHz or GHz range, it is very difficult to get a precise phase difference between input and output frequencies. Due to high input frequency, FD cannot be implemented in conventional static CMOS logic. Dynamic flip-flops are faster and more compact compared to static ones. In proposed work, a common dynamic flip flop variety True Single Phase Clock (TSPC) is used which performs flip-flop operation with high speed and low power [8]. The architectures of TSPC are based on edge triggering phenomena i.e. Positive and Negative. Among these two architectures, negative edge triggered architecture for dynamic latches are popular for high speed circuit design. In order to obtain sharp clock signals, NMOS devices are used as a stronger pull-down in negative edge triggered CMOS devices. In FD, first divider stage has maximum

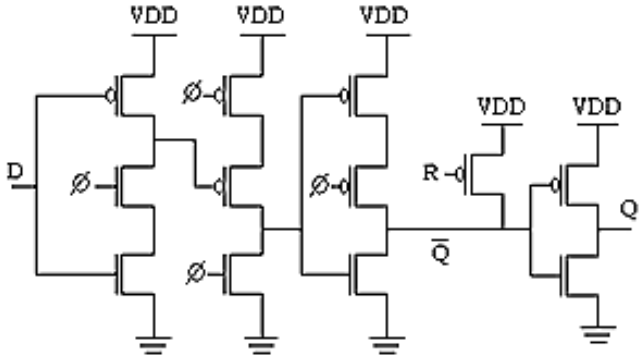


**Fig-7:** Negative Edge Trigger TSPC Flip-Flop

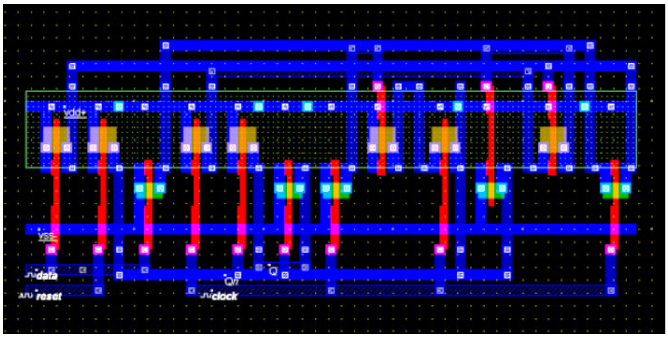

**Fig-8:** Layout of D-FF TSPC Flip-Flop in Microwind

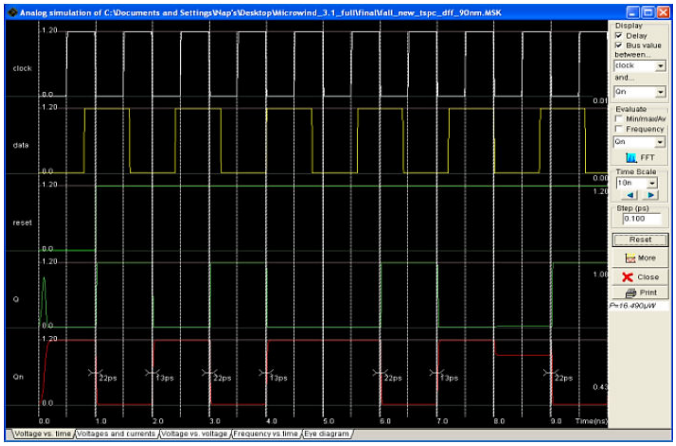

**Fig-9:** Simulation of D-FF TSPC Flip-Flop in Microwind

operating speed as FD has a high input frequency. As per the requirement, input frequency is divided by a fixed factor N. In this proposed work, divide by 2 network is made up of TSPC D-FF. This proposed FD reduces the power consumption and provide higher operating speed.

## 3. CONCLUSION

In this paper, 90-350 MHz Phase Locked Loop operating at 0.5V supply voltage is implemented in standard 90nm CMOS technology. The proposed Charge Pump reduces the leakage current by 60% and increases switching speed. Low voltage RO-VCO achieves high speed, wide tuning range and low KVCO gain. Proposed PLL can be used for most low power applications and can be used in wireless communication.

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