International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 03 Issue: 04 | Apr-2016 www.irjet.net p-ISSN: 2395-0072

Design and Comparative Analysis of Single Gate Tunnel FET and MOSFET

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Abstract - *The Tunnel Field effect transistor (Tunnel-FET) may be a new style of transistor. Although its structure is extremely kind of like a metal-oxide-semiconductor field-effect transistor (MOSFET), the basic shift mechanism differs. We know that MOSFET has many limitations so new technology is developed as Tunnel Field Effect Transistor (TFET). The tunneling field effect transistor uses the quantum-mechanical generation of carriers by band-to-band tunneling. It doesn't show the short channel effects just like the MOSFETs all the way down to a gate length within the vary of a multiple of the electron wave-length. This work elaborates comparison of different characteristics of MOSFET and TFET.In this paper we have designed and simulated a homo-junction n-Tunnel FET. We use Si, Ge, SiGe (with concentration Si=65%(0.65), Ge=35%(0.35)) as body and vary the gate material for getting better results. The simulation is done on licenced Cogenda TCAD software (Version 1.7.4). We have analysed transfer characteristics, output characteristics, C-V characteristics of all these devices. We compare ON current (I_{ON}), OFF current (I_{OFF}), Sub-threshold slope, Time delay, Transconductance, and PDP of these devices. ForSi-TFET, we got SS of 57.56 mV/dec, OFF-state current of 0.255896 pA/µm, ON-state current of 46.8133 µA/µm. The Tunnel-FET is very promising candidate for low power high speed application but their low ON current must be improved to be compatible with future VLSI circuits.*

Key Words:**MOSFET, TFET, band to band tunnelling, Power Delay Product (PDP), Visual TCAD.**

1.INTRODUCTION

MOSFET is basic building block of most integrated circuits because the MOSFET has become tinier, generation by generation, the chips supported it became a lot of quicker and fewer power hungry than their predecessors [13]. With the scaling of MOSFET, power supply should also be scaled down to reduce the power density. However, even within the ideal case of infinite gate capacitance, the SS of MOSFETs can't be reduced below 60mV/decade at room temperature. Other limitations of MOSFET are Channel Length Modulation, Short Channel Effects (SCEs), Velocity Saturation of Carriers, Impact Ionization, Narrow Channel Effect, Subthreshold Conduction [3]. The Tunnel Field Effect Transistor (TFET) measures asone of the foremost promising successors of Metal Oxide Semiconductor Field Effect Transistor (MOSFET) owing to their potential for sub-60mV/decade subthreshold swing. Such a reduced swing could be a necessary demand for ultra-low power, ultra-low voltage and high speed operation of next generation VLSI circuits. The gate controlled band to band tunneling is the working rule of the semiconductor unit and its basic structure could be a gated P-I-N diode. Compared to MOSFET, TFET has many merit of list; appropriate for low power applications, owing to lower leak current, higher immunity to short channel effects, subthreshold swing not restricted to 60mV/decade [19].

In this work, different TFETs with designs and characteristics are studied. This paper is organised as follows. Section II introduces working principle of TFET. In section III we have discussed our proposed methodology. Section IV represents simulation and results. Section V presents the conclusion.

2. PRINCIPLES OF TFET

Tunnel FETs utilize a MOS gate to manage the band-to-band tunneling across a degenerate tangency. The device is mostly OFF once zero bias is applied to the gate, the Conduction band minimum of the channel is above the valence band most of the supply, and therefore band-to-band tunneling is suppressed [20]. A tunneling window disclose as a result of the conduction band of the channel is shifted below the valence band of the supply. Electrons inside the valence band with energy throughout this tunneling window tunnel into empty states inside the channel and conjointly the transistor is ON [10].

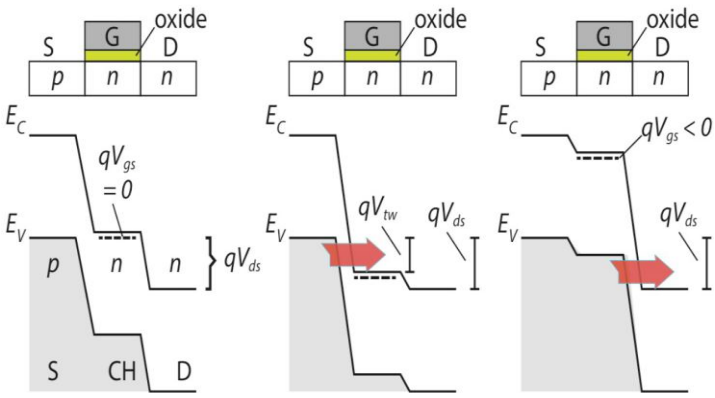

Fig -1: Schematic cross-section and energy band diagram of an n-channel TFET when the device is biased in (a) OFF (b) ON and (c) ambipolar state [10].

3. METHODOLOGY

We have done simulation in license Cogenda Visual TCAD software. We are designing and simulating MOSFET and TFET. We have used different body materials and compared with each other and to evaluate best performance among them. Tunnel FET required Band to Band tunneling model. We have used Kanes Band to Band tunneling model with A.BTBT= 3.9E+22 $eV^{-(1//2)}$ cm^{-1} $s^{-1}V^{-2}$ and B.BTBT= 2.25E+07 V $cm^{-1}eV^{-(2/3)}$ these parameters. We also used Lombardi mobility model. We have plotted I_D-V_G and C-V Characteristics of Si-TFET, Ge-TFET, SiGe-TFET to calculate various parameters like SS, PDP, Time delay, Transconductance, PDP, Time Delay, SS can be calculated using following formulas

$$PDP = C_G \times V_{DD}^2 \quad (1)$$

$$\text{Time Delay}(\tau) = \frac{Cg \times Vdd}{Ion} \quad (2)$$

$$SS = \frac{Vdd}{\log \frac{Ion}{Ioff}} \quad (3)$$

4. SIMULATION AND RESULTS

Below Fig. 2 shows the final device structure of TFET we have designed in the Visual TCAD for simulation. The parameter value used in design is as described in Table 1.

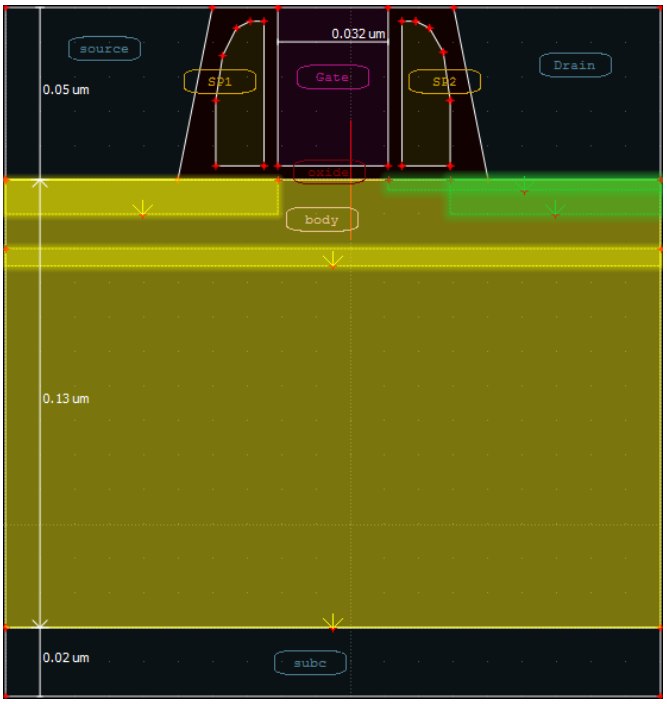

Fig -2: Device structure of TFET in TCAD

Table -1: Parameter & Values of TFET Used in TCAD Simulation.

Sr. No.	Parameter	Length	Material Used	Doping / Mesh Size
1	Gate	32nm	nPolySi	Mesh size= 0.003µm
2	Source	50nm	Al	1e+20 (Y=0.002) (Acceptor)
3	Drain	50nm	Al	1e+19 (Y=0.003)
			Lower Drain Doping	1e+18 (Donor)
4	Body	130nm	$Si_{0.65}Ge_{0.35}$	Mesh size= 0.005 µm 1e+17 (Acceptor)
5	Oxide	4nm	SiO_2	Mesh size= 0.004µm
6	Substrate	20nm	Al	Mesh size= 0.004µm
7	Spacer1 & Spacer2	18nm	Nitride	Mesh size= 0.004µm

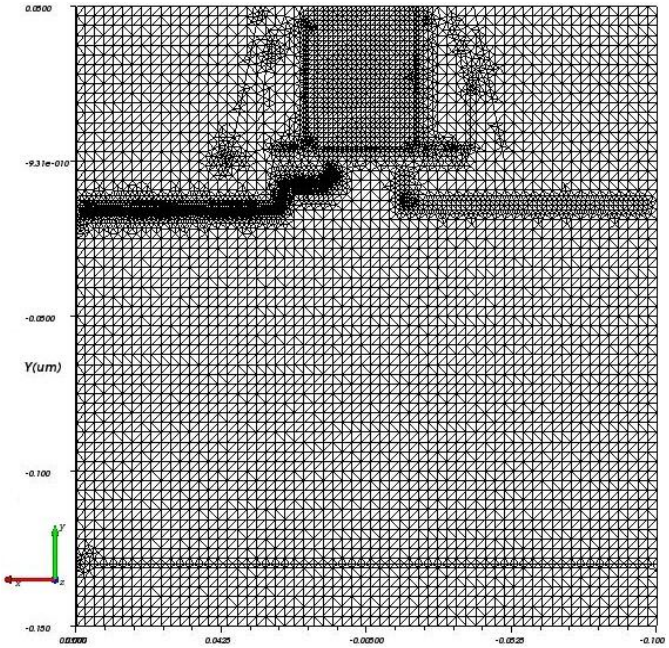

Fig -3: Mesh structure of the simulated Tunnel FET.

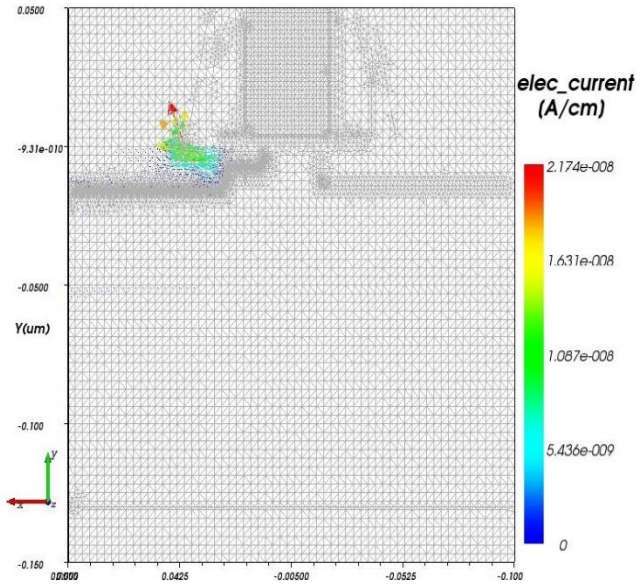

Fig -4: Flow of electron current in TFET at Vds = 1.2V.

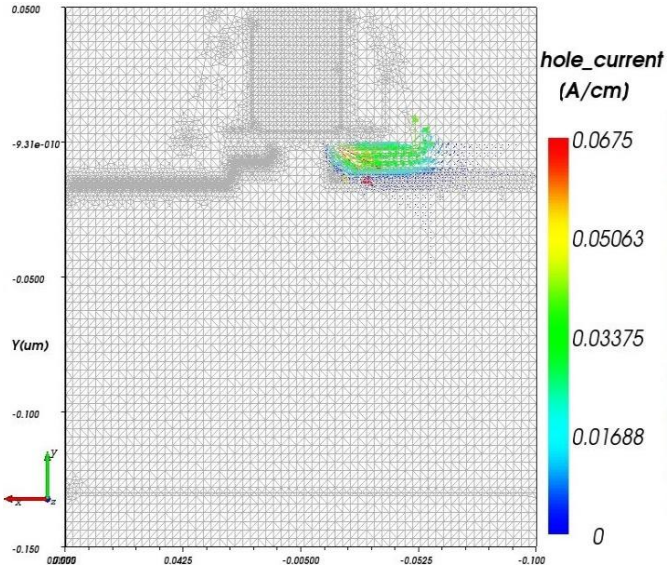

Fig -5: Flow of hole current in TFET at Vds = 1.2V

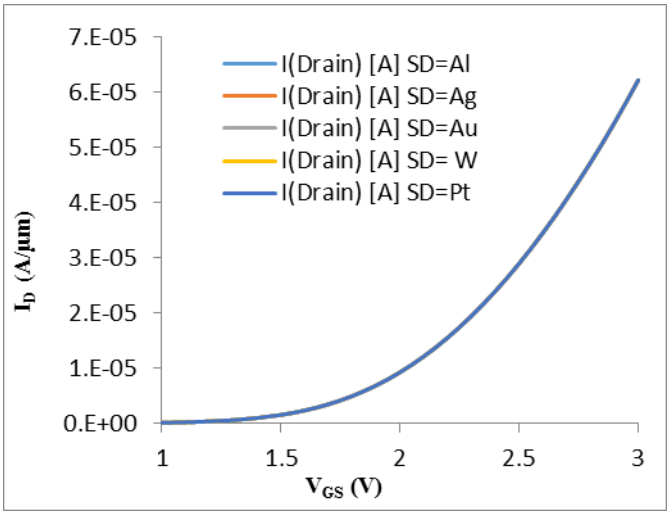

Fig -6: I_DV_G Characteristics for Al-Gate and Varying Source & Drain material

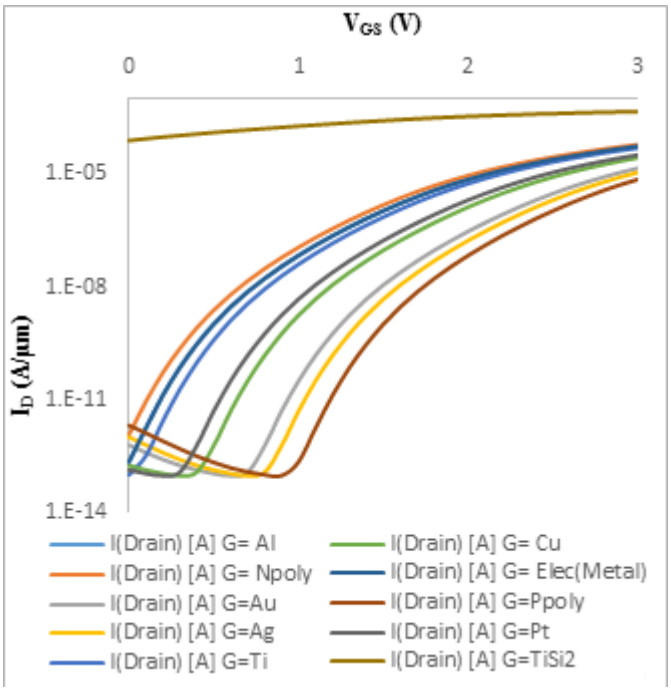

Fig -7:I_DV_G Characteristics for Source & Drain of Al and Varying Gate material

Material properties have various effects on device characteristics. Drain, Source and gate metal contact material should be a good conductor. Gate material has very significant effect on drain current which control the conduction channel, so we varied gate material keeping Drain & Source as Aluminium as varying Drain and Source doesn't affect the characteristics as shown in fig 6.

As shown in Fig.7 we use various gate material as Al, N-poly, Au, Ag, Ti, Cu, Elec, P-poly, Pt,$TiSi_2$ out of which N-poly gives better results among other materials.

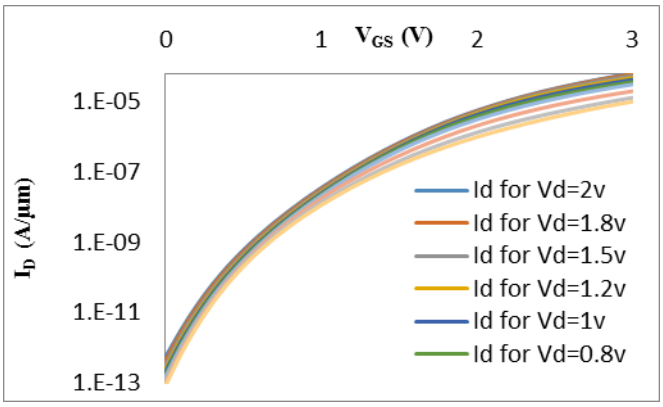

Fig -8:I_DV_G Characteristics of Si-TFET for various Vds in Log_{10} Scale.

Id-Vg characteristics for 0V <Vds< 2V of the 32 nm Npoly gate and Si-TFET is plotted on logarithmic scale. For Si TFET for Vds=1.2V, I_{off} = 2.55896e-13 (A/μm) at Vgs=0Vand I_{on}=4.68133e-05 (A/μm) at Vgs=3V.

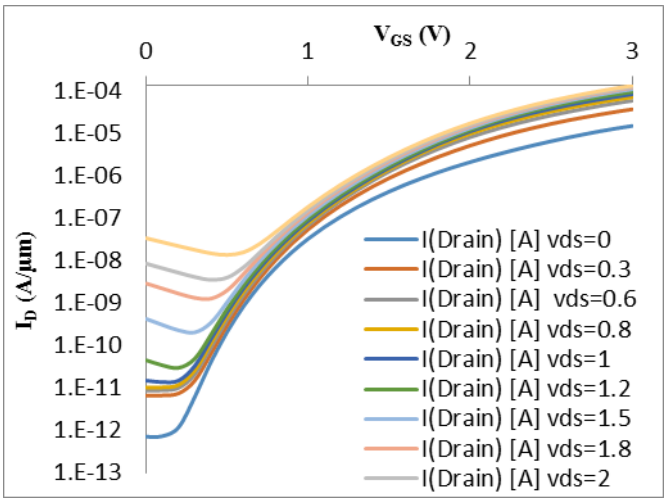

Fig -9: I_DV_G Characteristics of Ge-TFET for various Vds in Log_{10} Scale.

Id-Vg characteristics for 0V <Vds< 2V of the 32 nm Npoly gate and Ge-TFET is plotted on log scale. For higher gate voltage current gets saturated due to saturation of tunneling channel. For Ge-TFET for V_{ds}=1.2V I_{off} = 4.52214e-11(A/μm) at Vgs=0V and I_{on}=9.73722e-05(A/μm) at Vgs=3V.

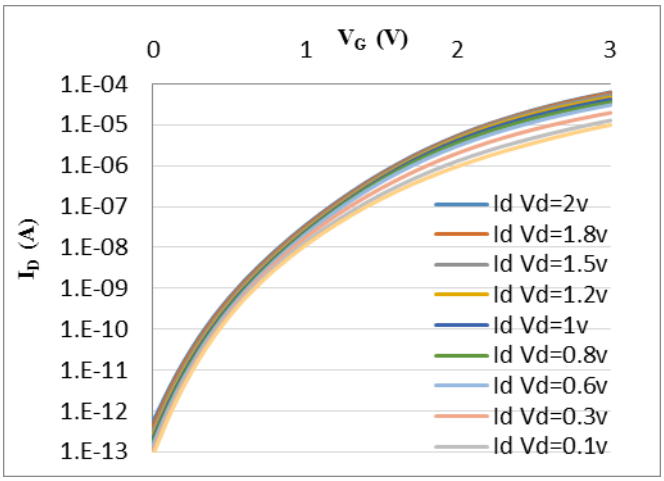

Fig -10: I_DV_G Characteristics of $Si_{0.65}Ge_{0.35}$-TFET for various Vds in Log_{10} Scale.

Id-Vg characteristics for 0V <Vds< 3V of the 32 nm Npoly gate and $Si_{0.65}Ge_{0.35}$-TFET is plotted on logarithmic scale. For SiGe TFET for V_{ds}=1.2V, I_{off} = 1.48351e-12 (A/μm) at Vgs=0Vand I_{on}=6.99737e-05 (A/μm) at Vgs=3V.

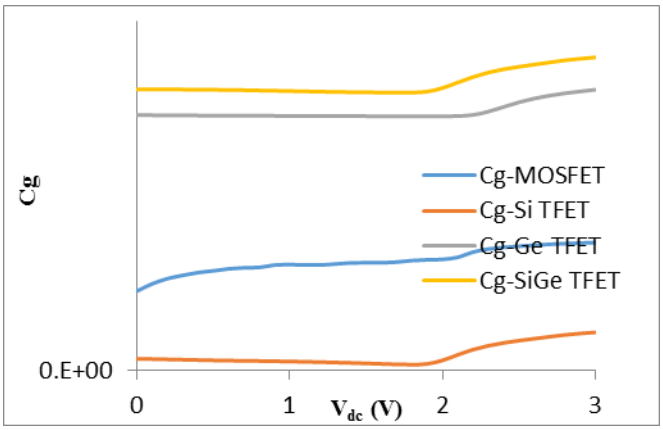

Fig -11: C-V Characteristics of MOSFET & TFET

Above Fig. 11 shows the C-V characteristics of MOSFET and TFET for different body material. The limiting issue for attaining high cut-off frequency is that the low price of trans-conductance and a high gate-to drain capacitance (C_{gd}). The dynamic behaviour of a device is that the results of device capacitive effects caused by the charges hold on within the device [21]. Simulated graph shows that Si-TFET has lowest capacitance whereas $Si_{0.65}Ge_{0.35}$ -TFET has very high capacitance.

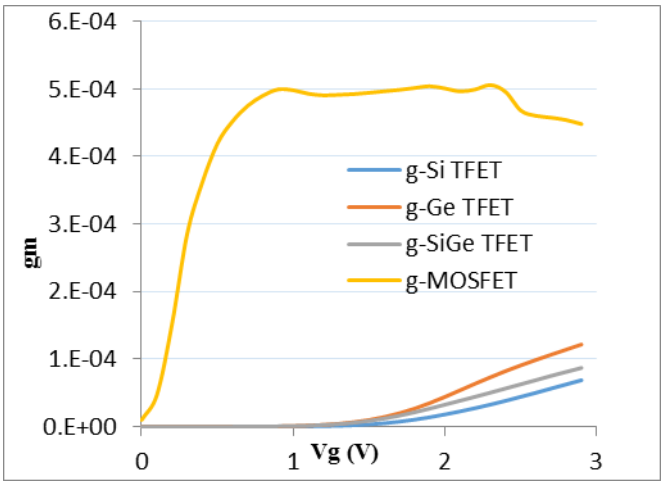

Fig -12:Transconductance of MOSFET & TFET.

Above Fig. 12 shows the Transconductance of MOSFET and TFET. Transconductance of MOSFET is very high as compare to the TFET. Above graph shows the transconductance (gm) for TFET of different material. As we have used Si, Ge and $Si_{0.65}Ge_{0.35}$ materials for body we have calculated Transconductance curve for these TFETS. We have compared these graphs and from these graph we can observe that transconductance of silicon TFET is lower than Ge TFET and $Si_{0.65}Ge_{0.35}$- TFET has values that is between these two.Comparative analysis results of MOSFET and TFET are as shown in Table 2.

Table -2: Comparison of Different Parameter of MOSFET and TFET V_{DD}=0.3V AND V_{DD}=1.2V.

Sr. No.	Device	I_{on} (A/µm) ↑	I_{off} (A/µm) ↓	Subthreshold Swing (SS) (mV/dec) ↓		Transconductance (gm) (S) ↑	PDP (J/µm) ↓	Time Delay (s) ↓
				V_{dd}=0.3 V	V_{dd}=1.2V			
1	MOSFET	**128.714e-05**	336348e-12	175.57	230	**4907e-7**	3.922e-16	**2.53894e-13**
2	Si TFET	4.68133e-05	**0.255896e-12**	**50.41**	214	7.97e-07	**3.183e-17**	5.666235 e-13
3	Ge TFET	9.73722e-05	45.2214e-12	71.76	329	27.52e-07	9.449e-16	80.86858 e-12
4	$Si_{0.65}Ge_{0.35}$ TFET	6.99737e-05	1.48351e-12	**57.56**	227	25.74e-07	1.036e-15	123.3240 e-13

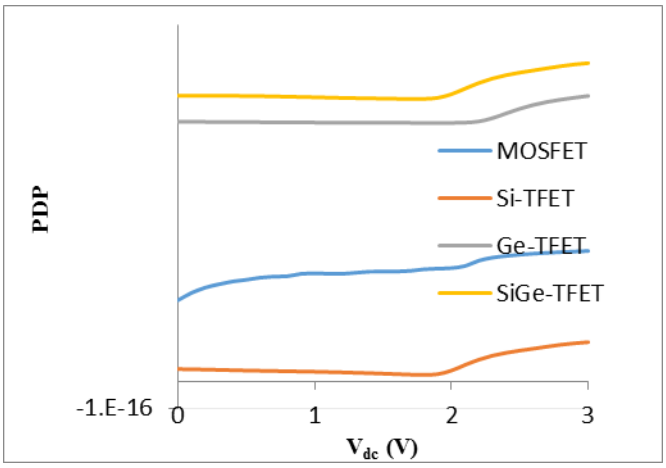

Fig -13: PDP of MOSFET & TFET.

Power Delay Product gives us how much power is consumed by the device at that particular delay. Combining these two parameters is important as these are the main performance parameters of the device.

5. FUTURE SCOPE AND CONLUSION

This work has been analysed thoroughly about the subthreshold swing performances of advanced Tunnel FET devices of 32nm gate length with the MOSFET. The TFET has lower OFF-current than the traditional MOSFET, each TFET type that is simulated have comparatively similar low ON-current thus increasing the ON-current may be a huge challenge ahead.For the TFET there is still a need to both further decrease SS and increase I_{ON} to be a competitive replacement for the conventional MOSFET. By increasing the source doping it becomes possible to increase the overall tunnel current.

To satisfy the requirement of I_{ON} current according to ITRS low band gap material for source high doping concentration required. Also further Hetro-structure can be used to get steep subthreshold slope and high I_{ON}. Ambipolar behaviour of TFET can be reduced using thick buried oxide layer.

6. CONCLUSIONS

In this work, performance of TFET is analysed andstudied.We have proposed and mentioned the fundamental static operation, and simulated the characteristics of tunnel FET. TFET has lower sub-threshold slope than MOSFET. Tunnel FET is applicable for low power devices as it gives lower off current. It is difficult to achieve high I_{ON} degrading I_{OFF}, and sub-threshold slop below 60mV/dec. Main disadvantage of Si-TFET is that the ON current is very low so we don't satisfy the ITRS ON current value. Which is not compatible with current CMOS based circuits. So we changed Si body with Ge and $Si_{0.65}Ge_{0.35}$ compound material which are low band gap material, which reduces tunneling distance at source channel junction. But improvement in ON current is not observed. In-spite of these drawback of TFET, it is promising candidate for future low power applications. Therefore main focus for TFET device is to improve the ON current so thatit can fully replace the conventional MOSFET technology in future VLSI circuits.

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