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Using VLSI for Full-HD Video/frames Double Integral Image Architecture Design of Guided Filter

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Abstract - In image and video processing filtering is the one of the technique which is mostly used. By considering the content of guidance image the guided filter computes the filtering output. Which is used as edge-preserving smoothing operator like the bilateral filter. Like the popular bilateral filter the guided filter can be used as an edge-preventing smoothing operator. For achieving the computational demand of guided filter in full HD video, a double integral image architecture for guided filter ASIC design is proposed in this paper. Also the hardware architecture is proposed later to achieve real time HD application. In which the design can operate at 100 MHz For FULL-HD 30 frames/s with 3.2 KB on chip memory.

Key Words : Guided filter, edge preserving bilateral filter, integral image, double integral image architecture

1.INTRODUCTION

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In computer vision, computer graphics, computational photography, etc. Filtering is an image processing technique widely used. filtering can be applied in many applications such as noise reduction, texture editing, detail smoothing/enhancement, colorization, relighting tone mapping, haze/rain removal, and joint up sampling. The edge-preserving bilateral filter is mostly used [1]. Liu *et al.* [2] applied bilateral filter to image noise reduction and Durand *et al.* [3] used bilateral filter on high dynamic range (HDR) images. Based on bilateral filter, joint bilateral filter is developed in [4] in flash/no-flash de-noising. Kopf *et al.* [5] used joint bilateral filter for up sampling problems. due to its computation efficiency and memory concern bilateral filter, real-time implementation [6] usually adopts histogram-based approximation. For real-time filter applications on HD videos Guided filter has the non-approximation characteristic and offers an ideal option. the guided filter is a non-approximate linear-time algorithm, many applications adopted a guided filter as the filtering method. He *et al.* [9] further to improve the alpha mask used a guided filter at the post-processing step Ding *et al.* [10] under the guidance of the original image a guided filter used to filter out the image saliency. In [11] , a guided filter was used for fast cost volume filtering because of the degradation in quality caused by fast approximation bilateral filter. In [12], guided image filtering was used to smooth the result of transferred colours in order to suppress colour noise while preserving colour structures, Zhang *et al.* [13] used guided filter to refine the crude transmission map. Guided filter has high computational load since it has to filter the transmission map at every frame. In [14], to propagate the value from edge locations into the unknown region by using the blurry image as the guided image a guided filter was applied. Hosni *et al.* [15] For some applications mentioned above, a high throughput guided filter is needed. applied a guided filter to 3-D spatial temporal space for computing temporally coherent disparity maps. However, it is not applicable for CPU computation. Although GPU provides an alternative solution to a high-throughput guided filter, it has higher cost and power demand that is not suitable for mobile devices like digital cameras or mobile phones. Therefore, in this paper VLSI architecture design of guided filter is proposed.

2.Guided filter Preparation and challenge

For the preparation and designing the guided filter on should know all the equations needed in designing Given a guidance image I and an input image p, a filtered output image q can be produced by guided filter. There is a key assumption of guided filter: The output image q is a local linear transformation from the guidance image I. That is, an output pixel qi is a linear transform of guidance image I in a window wk cantered at pixel k

$$qi = ak\, Ii + bk, \forall i \in wk \quad (1)$$

where ak and bk are linear constant coefficients in window wk. .Since $\nabla q = a\nabla I$, the output image q has edge only if the guidance image I has edge. In order to find the appropriate coefficients.

To determine the linear coefficients ak;bk, we need constraints from the filtering input p. We model the output q as the input p subtracting some unwanted components n like noise/textures

$$qi = pi - ni$$

$$E(a_k, b_k) = \sum_{i \in \omega_k}((a_k I_i + b_k - p_i)^2 + \epsilon a \quad (2)$$

The parameter here prevents *ak* from becoming too large. The solution of *ak* and *bk* for above cost function are as

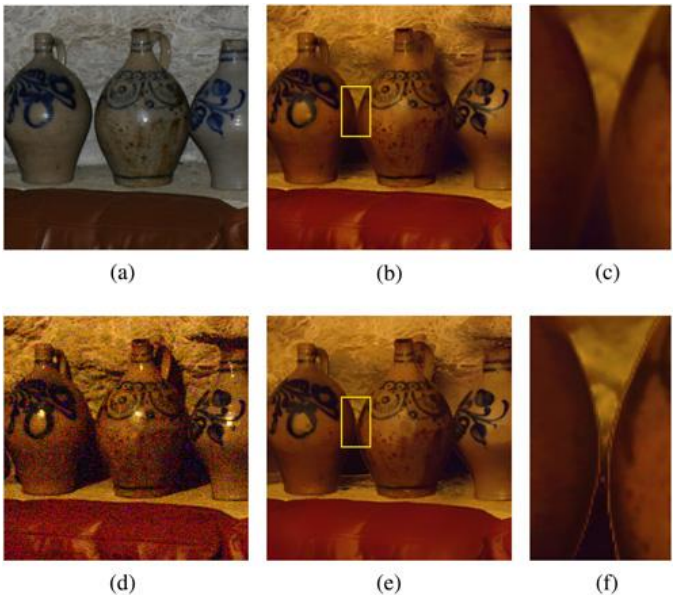

Fig. 1. Comparison of guided filter and joint bilateral filter by flash/no-flash De noising. In the result of joint bilateral filter, gradient reversal artefacts are noticeable near some edges, as shown in (f). (a) Guidance *I*. (b) Guided filter. (c) Crop. (d) Filter input *p*. (e) Joint bilateral filter. (f) Crop.

$$b_k = p_k - \bar{a}_k \mu_k \quad (3)$$

In the window |*w*| is the number of pixel *wk*, *μk* and *σk* 2 are the mean and variance of *I* in window *wk*, and $p^{-}k$ is the mean of input image *p* in window *wk*. After the coefficients are well defined, the next step is to calculate all the local windows in the whole image. However, for any pixel *i*, it may have different output pixel value *qi* calculated by different local windows. An average process isadopted for pixel *i*, which is defined as

$$q_i = \frac{1}{|w|}\sum_{k:i \in \omega_k} a_k I_k + b_k = \bar{a}_i I_I + \bar{b}_i \quad (4)$$

The computations of the sum of windows and averages in (4) can be efficiently accelerated by an integral image, which greatly reduces the computational complexity. Based on the data in [8], for a gray-scale optimized guided filter, for 30 frame/s full-HD (1920×1080) videos is not fast enough for processing a 1-MP image on a PC needs 80 ms. Therefore for the computation of the guided filter , a hardware architecture is proposed to accelerate the computation The memory demand for guided filter is 4 + 2×1920×1080×4 = 49, 766, 400 _ 49.77 MB. (Here counts for integral images of *I*, *I*2, *p*, *Ip*, *a*, and *b* at single precision.)

There are many challenges in the design are the designing of the guided filter For a full-HD frame, even adopt the integral image approach, there are total three challenges we are having.

The first challenge is how to use on-chip memory practically and the main important issue is how to reduce the memory by saving all integral images in off chip memory so that the bandwidth should have to reduce. for reducing the bandwidth we are using double integral image architecture for the guided filter to solve the problem between on chip memory and bandwidth.

As we seen earlier there are many challenges in designing of the guided filter in that The second challenge is trade-off between design complexity and the total gate count. Using the single precision data format makes the system easier to design it takes more bits to store data, which means the size of on-chip memory increases sharply

The third designing issue is a boundary handling issue. Tseng *et al.* [6] proposed a novel architecture for integral histogram, but the lower boundary (last few rows) for each frame is neglected. To solve the boundary problem of the integral histogram for last few rows is solved by Tseng which we are extending in the proposed architecture of the double integral image for full HD video using VLSI.

3.Design of Hardware Architecture

Fig. 2 shows the proposed architecture design of the guided filter which consist of the . The design consists of six integral image engines on chip dynamic RAM which is connected through the bus with the other remaining part of the architecture design. Also it consist of one coefficient kernel engine, and one output kernel engine. also it consist of six integral image engine for which called as a IIE. The histogram calculation of the IIE Engine is proposed in [6].As we are concentrating on the double integral image architecture we are not giving more importance to the IIE that is integral image engine the novelties of this paper the design of coefficient (*ak*,*bk*) and output (*qi*) kernel engine, and the double integral image architecture for the guided image filter. For the hardware there are 4 steps first is giving the input video format is full-HD (1920×1080), 30 frame/s. and the operating frequency is 100 MHz required for the implementation of the guided filter. as implementing the guided filter a prototype IO wrapper is used(needed) in between the ASIC design and the bus .the IO controller or IO wrapper is used in second stage of the architecture which is depend upon the parameter that is on the type of the bus that are chosen by the user and the parameter of the guided filter. By modifying the hardware Parameters proposed architecture can be also applied to different

specifications The user can use the proposed architecture for guided filter to implement the customised IP as per their requirement.

The design consist of the stripe-based method proposed in [6], which a frame can decompose into several vertical stripes. Therefore, the integration and extraction process of each stripe can be done, the required memory reduces from the width of frame to the width of stripe plus the extended region.

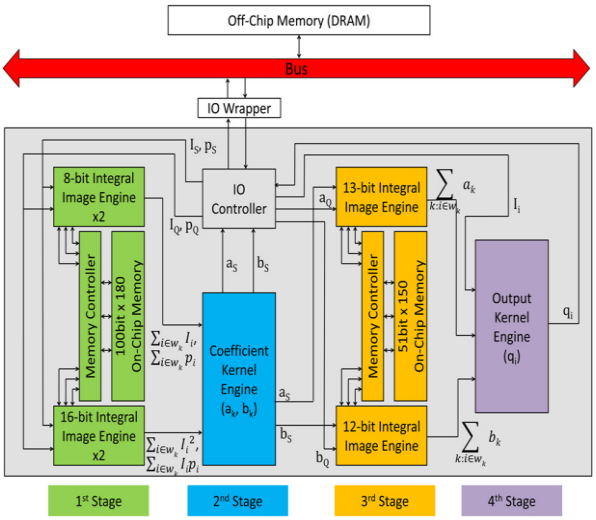

Fig. 2. Proposed architecture of guided filter with double integral image..

4.Double Integral Image Architecture

The use of the double integral images for rapid feature evaluation become popular with the face detection algorithm[18]A guided filter can be implemented by the integral image method, it is impossible to store the intermediate coefficients *ak* and *bk* in on-chip memory due to its large memory demand. Based on the integral histogram architecture proposed in [6] , a double integral image architecture is proposed,. The data flow of double integral image architecture can be separated into two parts. In the following, the whole dataflow will be introduced . First part of dataflow of the proposed double integral image architecture. And Second part of dataflow of the proposed double integral image architecture. The right-most part shows the relationship of output qi and corresponded pixel location in the input stripe.

A. Dataflow of Double Integral Image Architecture

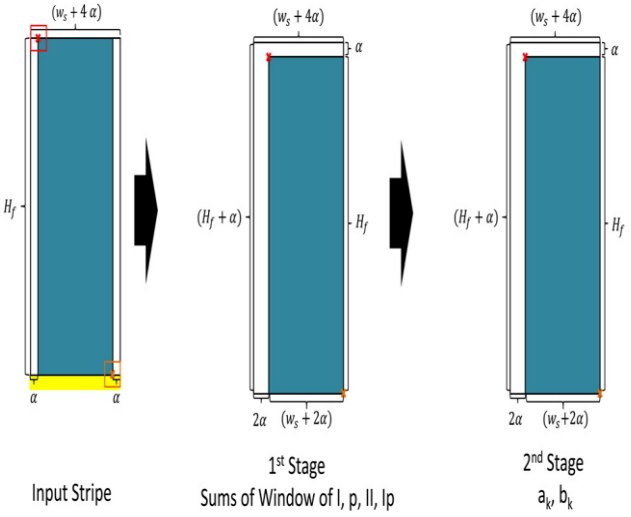

Fig. 3. First part of dataflow of the proposed double integral image architecture.

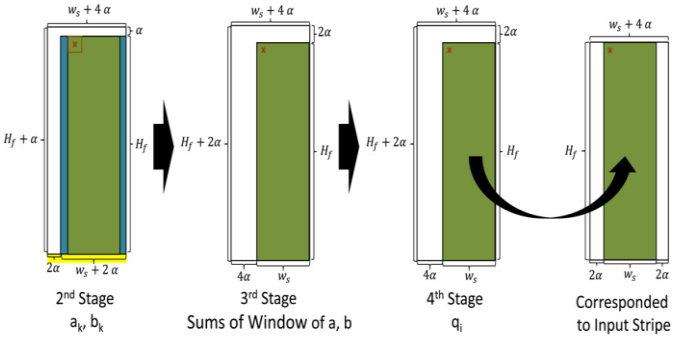

Fig. 4. Second part of dataflow of the proposed double integral image architecture. The right-most part shows the relationship of output qi and corresponded pixel location in the input stripe.

The first part is illustrated in Fig.3. The first and second stages here are referred to the same stages as in Fig.2(Proposed architecture of guided filter with double integral image.). The input data is only a stripe rather than a full frame due to the stripe-based method. In order to reduce the on-chip memory for the storage of *a* and *b*, at the second stage, the outputs *a* and *b* are written to a small buffer at the off-chip memory. The required off-chip memory size is,

$$|S|\times(ws + (|S|-1))\times(wa + wb)$$

where *wa* is the bit number of *a* and *wb* is the bit number of *b*. The second part of the dataflow is illustrated in Fig. 14. In the second stage, the available data is the blue area. brown square in the input second stage. Given the sums of window of *a* and *b*, the output *q* can be calculated at the fourth stage.it is derived as follows;

$$(x0, y0) == (x4 - (|S| - 1), y4 - (|S| - 1))$$

where $ws + 2(|S| - 1) > x4 \geq 2(|S| - 1)$, $Hf + |S| - 1 > y4 \geq |S| - 1$ or $ws + |S| - 1 > x0 \geq |S| - 1$, $Hf > y0 \geq 0$.

This correspondence is also illustrated in the right-most part of Fig.4.

Table 1 given below shows the Resource used by Different Architecture of Guided Filter Per Frame in which it can be seen that the comparison of the off chip memory specifications in direct method the memory is of 51.58MB,whereas for the single integral image the memory is 6.48MB.Also for the proposed double integral image it is of the 14.53KB that the conclusion can be made that the memory required for the proposed architecture required is less. Also can see the difference between the bandwidth used that is for proposed design it required only 262.31MB which is less as compare to the direct method and the integral method.

TABLE I

Resource used by Different Architecture of Guided Filter Per Frame

	Direct Method	Single Integral Image	Proposed Double Integral Image
Off-chip Memory	51.58MB	6.48MB	14.53KB
Bandwidth	2.13Gb	327.11Mb	262.31Mb

The implementation result and chip layout are shown in Table II Our specification of Guided filter is operating at 100MHz frequency and 30 frame/s full-HD (1920×1080). The proposed guided filter architecture is implemented with TSMC 90 nm 1P9M technology in which can know the chip size, core size also the power consumption and the gate count which is 92.895

TABLE II

Technology	TSMC 90nm CMOS Mixed Mode Signal MS General Purpose LowK Cu 1P9M
Frame Size	1920×1080
Frame Rate	30
Filter Window Size	31×31
Stripe Width	120
Operating Frequency	100MHz
Chip Size	1.46×1.43 mm^2
Core Size	0.92×0.89 mm^2
Power Consumption	22.522 mW
Gate Counts	92,895
On-Chip Memory (Byte)	3,206

5. RESULT OF IMPLEMENTATION

In the section of result implementation, our implementation result is presented and compared with other previous works .previously used filter is Bilateral filter instead of Guided filter which is operated on TSMC 0.18 μm and the frame size is 320×240 on the rate of 144 at the operating frequency of 60 MHz and the Throughput of the pixel is 11M with a gate count of 355K and 7.8K on chip memory. Also previously used filter is Joint Bilateral filter instead of Guided filter which is operated on USM 90 Nm and the frame size is 1920×1080 on the rate of 30 at the operating frequency of 1000 MHz and the Throughput of the pixel is 62M with a gate count of 276.2K and 23K on chip memory. Our specification of Guided filter is operating at 100MHz frequency and 30 frame/s full-HD (1920×1080). The proposed guided filter architecture is implemented with TSMC 90 nm 1P9M technology. The implementation result and chip layout are shown in Table II

TABLE III

Comparison with Other ASIC Filter Implementations

	Han [16]	Tseng [6]	Proposed
Filter Type	Bilateral Filter	Joint Bilateral Filter	Guided Filter
Technology	TSMC 0.18um	UMC 90nm	TSMC 90nm
Frame Size	320x240	1920x1080	1920x1080
Frame Rate	144	30	30
Filter Window Size	11x11	31x31	31x31
Operating Frequency	60 MHz	100 MHz	100 MHz
Throughput (Pixel/s)	11M	62M	62 M
Gate Counts	355K	276.2K	92.9K
On-Chip Memory (B)	7.8K	23K	3.2K

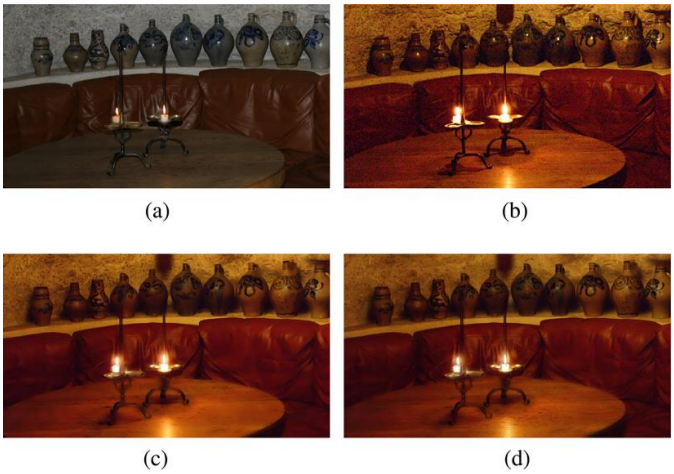

Fig. Comparison of the filtered result of the proposed architecture and the filtered result of software in double precision by flash/no-flash denoising. (a)Guidance I. (b) Filter input p. (c) Filtered result of software in double precision. (d) Filtered result of the proposed architecture.

Above figure gives the comparison of the filtered result by the VLSI architecture and the filtered result of software in double precision by denoising fig(a)shows the guidance image I fig(b)filtered result given by the software in the process of double precision and last but not the least the fig(d)gives the final output image that is the filtered result of the proposed architecture that is the VLSI implementation of the guided filter.

6.CONCLUSION

The proposed paper is for a VLSI architecture design for guided filter. With the proposed architecture, an example design has throughput of 30 frame/s full-HD (1920×1080) with 92.9K NAND gates and 3.2KB on-chip memory is implemented. Compared with other previous filter , the proposed guided filter technology reduces not only gate counts but also on-chip memory, and still has high throughput. Using of guided filter can save hardware cost without the loss in quality. Now as the coefficients are only calculated for gray-scale guidance image (*I*). By modifying the coefficient kernel in the second stage, the proposed architecture can handle colour images.

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