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Five Level Active Neutral Point Clamped Converter based STATCOM

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Abstract - *Harmonic voltages and currents in an electric power system are a result of non-linear electric loads. Usually a STATCOM is installed to support electricity networks that have a poor power quality. In this work, a multilevel Active neutral point converter with separated dc capacitors which is driven by carrier-based pulse width modulation to implement in the STATCOM is proposed. Active NPC (ANPC) improves the loss distribution of NPC by replacing diodes with active switches providing alternative neutral point path. A PID controller is designed to obtain the desired level of the output. This application is designed in the MATLAB/ Simulink platform. With the phase-shifted carrier based scheme, natural balancing can be achieved in a straight forward manner. However, to achieve natural balancing with the optimum harmonics, phase-disposition (PD) carrier-based scheme which use the (n – 1) carrier signals is proposed. The relationship between the average neutral-point current and zero sequence voltage is investigated, and an optimum zero-sequence voltage is calculated to regulate the neutral-point potential.*

Key Words: Active Neutral Point Clamped converter, Phase disposition pulse width modulation, Total Harmonic Distortion

1. INTRODUCTION

The AC power transmission line operation is generally constrained by limitation of one or more network parameters which includes line impedance and operating variables such as voltages and currents. As a result, the power line is unable to direct power flow among generating stations. Flexible AC Transmission System (FACTS) is the technology; its principal role is to enhance power transfer capability and controllability in AC power system. A static synchronous compensator (STATCOM) is a regulating device can act as either a source or sink of reactive AC power to an electricity network.

The multilevel inverters have drawn tremendous interest in the power industry. They provide a new set of features that are well suited for use in reactive power compensation. The concept of Multilevel Inverters (MLI) does not limit on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other in order to create a smoother stepped waveform, with lower dv/dt and lower harmonic distortions. With the more voltage levels, the waveform it creates becomes smoother, but with many levels the design becomes more complicated, with more components and complicated controller for the inverter is needed.

ANPC inverter is one of the hybrid topologies to overcome the drawbacks of DCMC and FC based inverters. The diodes in the DCMC are replaced with active switches. Then the capacitors of the flying capacitor based inverter are minimized. There are several technologies available for the switching of these MLIs. Among them SVPWM will produce better harmonic reduction [12]. The SPWM techniques for MLI are analyzed. Among which PDPWM will produce better results when compared with phase shifted techniques as well as other level shifted techniques [6], [9], [11] and [10]. The PDPWM technique is used for various converters [1], [2] and [7]. SHE modulation for harmonic elimination also analyzed [3]. Hybrid PWM by combining two or more technique also used [4] and [13]. Various converters are used for STATCOM design [8].

Analysis of various modulation Techniques the PDPWM technique will produce better efficiency, harmonic reduction and loss distribution. The STATCOM is designed with the five level ANPC converter and triggered with PDPWM technique in MATLAB/ Simulink tool.

2. MULTILEVEL ANPC CONVERTER BASED STATCOM

Five-level active neutral-point clamped (ANPC) converter is an attractive multilevel topology, which is more suitable for high-performance medium-voltage motor drives. Its dc-link is subdivided into two parts and only four switches and one FC are needed for clamping per phase; hence, the costs, volume, and control complexity can be reduced. A phase-disposition PWM (PD-PWM) with zero-sequence voltage injection method was proposed in to control the NP potential of the 5L-ANPC converter. The redundant switching states are utilized to control the voltages across the FCs.

However, the calculation and selection of zero-sequence voltage is very complex and the switching frequency is not constant for the outside switches with PD-PWM. In, a control strategy based on selective harmonic elimination PWM was proposed and the voltage across the FCs was balanced by swapping the switching patterns. The NP voltage was regulated by adding or subtracting a relatively small pulse to the switching pulse signals. This method is very suitable for the high power and low switching-frequency applications. However, the voltage regulation ability is not strong due to the low switching frequency and the capacitor voltage ripple will be high.

The one phase leg of three phase five level Active Neutral point clamped converter is shown in Fig 1. The most essential problem of 5L-ANPC inverters is how to maintain the DC-link capacitor voltages balanced.

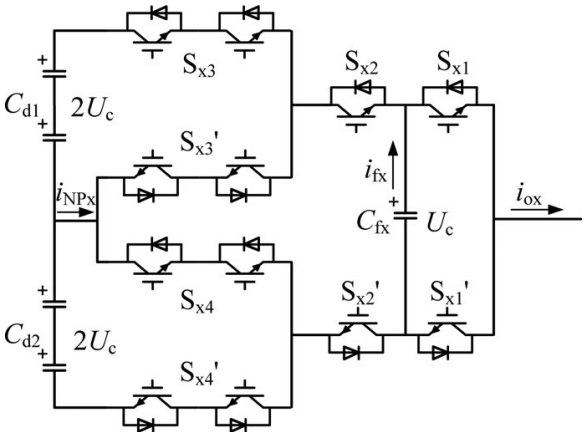

Fig-1: Single phase leg of five level ANPC converter

PD PWM is commonly used in multilevel converters and can achieve multi-objective optimization easily by zero-sequence voltage injection, which is more suitable for converters with high voltage levels.

3. SYSTEM CONFIGURATION OF STATCOM

In the block diagram Fig 2, the STATCOM is designed with the Active Neutral Point Clamped converter. Phase Disposition Pulse Width Modulation is chosen as the modulation technique. Thyristor switching devices are used for the converter. Here the MOSFET to control the injected current or the compensating voltage. DC link capacitance value has to be chosen. The number of the switching devices in the ANPC converter and the number of the capacitors are decided by the level of the inverter chosen. Here five level ANPC converter is chosen and so the number of switching devices used is 12. Here no switching diodes are used to minimize the switching losses as well as to increase the efficiency. Phase Disposition modulation has to be designed according to the level of the converter used. That is for m level of inverter the number of carrier signals used is m-1. So here for the five level inverter four carrier signals are used to achieve the required output.

A constant source is connected to the load through the converter/inverter circuit. The inverter block is made of IGBT (Gate-insulated bipolar transistors). To provide proper quality of power to the load and also to reduce the harmonics the STATCOM is connected as the shunt compensating device. STATCOM connected will provide compensation current for the equalization of the voltage quality. Therefore the current harmonics can be eliminated. The injection of the current depends upon the switching sequence of the active neutral point clamped converter. The PDDWM will provide better equalization of the voltage when compared with the other SPWM.

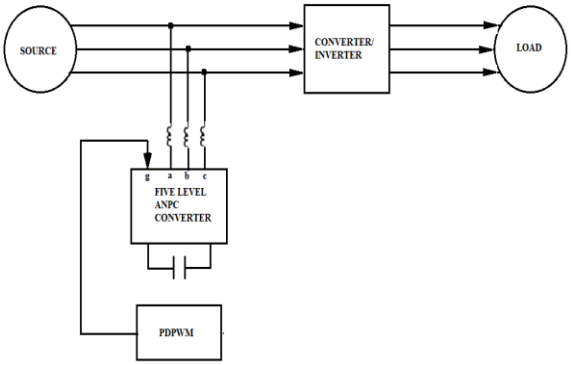

Fig-2: Block Diagram of STATCOM

Since IGBT devices are used in the three phase inverter, the generation of gate pulse is required. The method used for the triggering of the inverter is pulse width modulation. In the PWM technique for gate pulse generation the voltage regulator block and the Discrete PWM blocks are employed.

For a five level converter, this technique requires four carrier signals which are triangular in nature and the reference signal is of sinusoidal. Here all carrier signals are in phase but level shifted. In phase disposition method all the carriers have the same frequency and amplitude. Moreover all the N-1 carriers are in phase with each other. It is based on a comparison of a sinusoidal reference waveform with vertically shifted carrier. This method uses N – 1 carrier signals to generate N level inverter output voltage. All the carrier signals have the same amplitude, same frequency and are in phase. In this method four

triangular carrier waves have compared with the one sinusoidal reference wave. The PD-PWM is applied and the voltage balance is performed by a proper selection of redundant switching states by using neutral point potential balancing algorithm. The NP potential balancing algorithm is implemented.

4. OPERATION OF STATCOM

All the switching states V0–V7 are listed in Table 1, where i_{cf} and i_{NP} are the corresponding floating capacitor current and NP current of each switching state and i_o is the phase current. The neutral-point of the dc-link is referred as the zero potential. When the phase current i_o is positive, switching state group G1 can be used to discharge the floating capacitor while G2 can be used to charge it.

Table-1: Switching states of 5L-ANPC inverter

S1	S2	S3	S4	S5	S6	V_O	i_{cf}	i_{np}	Switching State
0	0	0	0	0	0	$-U_{dc}/2$	0	0	V0
0	0	0	0	0	1	$-U_{dc}/4$	i_0	0	V1
0	0	0	0	1	0	$-U_{dc}/4$	$-i_0$	i_0	V2
0	0	0	0	1	1	0	0	i_0	V3
1	1	1	1	0	0	0	0	i_0	V4
1	1	1	1	0	1	$U_{dc}/4$	i_0	i_0	V5
1	1	1	1	1	0	$U_{dc}/4$	$-i_0$	0	V6
1	1	1	1	1	1	$U_{dc}/2$	0	0	V7

It can be noticed that voltage levels $-U_{dc}/4$ and $U_{dc}/4$ each corresponds to two redundant switching states with different effects on the floating capacitor. For voltage level $-U_{dc}/4$, switching states V1 and V2 generate the same voltage level with reverse i_{cf}. For voltage level $U_{dc}/4$, switching states V5 and V6 generate the same voltage level with reverse i_{cf} as well. Therefore, all the switching states can be divided into two groups: G1 and G2.

Table-2 : Switching state groups used for voltage balancing of floating capacitors

Voltage deviation	Phase Current	Switching States	Group
$\Delta U_f>0$	$i_0>0$	V0, V1, V3, V4, V5, V7	G1
	$i_0<0$	V0, V2, V3, V4, V6, V7	G2
$\Delta U_f<0$	$i_0>0$	V0, V2, V3, V4, V6, V7	G2
	$i_0<0$	V0, V1, V3, V4, V5, V7	G1

As shown in Table 2, V1 & V5 are used in group G1 and V2 & V6 are used in group G2, where ΔU_f is the deviation of floating capacitor voltage from its reference value. When the phase current i_o is negative, switching state group G1 can be used to charge the floating capacitor and G2 can be used to discharge it. So, according to the polarity of ΔU_f and i_o, by properly selecting the switching state group for each phase, the floating capacitor voltage can maintained balanced within a limited margin of its reference value. The NP potential is also affected by the redundant switching states shown in Table1. However, it cannot be controlled by selecting redundant switching states directly like floating capacitor. Other more accurate control methods should be pursued.

5. NEUTRAL POINT POTENTIAL BALANCING METHOD

PDPWM requires four carriers of the same amplitude, frequency and phase which are arranged into contiguous bands that fully occupy the linear modulation range. A reference sinusoidal modulation signal is compared with the four triangular carriers to define the voltage level that has to be generated at the output. This strategy is spectrally superior to other carrier layouts because it produces large harmonic concentration at some specific frequencies that cancels in the line-to-line voltages, hence reducing the output harmonic distortion. However, PDPWM does not provide natural capacitor voltage balance. Therefore, an active balancing scheme IS required to stabilize the FC voltages to the desired levels

Before considering the NP potential balancing of 5L-ANPC inverter, we must confirm that the NP potential balancing can be achieved. It is clear no matter which modulation scheme is adopted, the NP current is the primary variable which determines the variation of NP potential. Once the neutral current is known, the NP potential variation can be obtained. If $U_{dc}/4$ is selected as the base voltage value, then the range of the reference phase voltage is $-2 \le u_x \le 2$, where x represents phase **a**, **b** or **c**. The output voltage levels $-U_{dc}/2$, $-U_{dc}/4$, 0, $U_{dc}/4$ and $U_{dc}/2$ are numbered from − 2 to 2, respectively. In the sinusoidal pulse width modulation scheme, the output voltage jumps between two voltage levels during every carrier period. If the carrier frequency is high enough, then the reference voltage can be regarded as a constant during a carrier period. The duty cycle of high- and low-level is determined by the reference voltage u_x and can be obtained as follows. When $k-1 \le u_x < k$ (k = –1, 0, 1 or 2), the duty cycle of voltage level k is:

$$d_x^k = u_x - k + 1, \quad u_x \in [k-1, k) \qquad (1)$$

when $k \le u_x < k+1$ (k = –2, –1, 0 or 1), the duty cycle of voltage level k is:

$$d_x^k = k + 1 - u_x, \quad u_x \in [k, k+1) \qquad (2)$$

where k is the voltage level –2, –1, 0, 1 or 2.

5.1. Demanded average NP current

Although the NP potential can be naturally balanced under ideal and steady conditions, it also may diverge under non-ideal and dynamic conditions if not controlled. Define the NP potential deviation is

$$\Delta U_{NP} = (U_{d2} - U_{d1})/2, \quad (3)$$

where U_{d1} and U_{d2} are the voltages of upper and lower dc-link capacitors, respectively. In order to maintain the NP potential balanced and eliminate its offset, an average NP current is expected to be injected into the neutral point. If the two dc-link capacitors have the same capacitance, the demanded average NP current in a carrier period can be written as:

$$i_{NP,ref} = -2C \frac{\Delta U_{NP}}{t_p} \quad (4)$$

where C is the capacitance value of C_{d1} and Cd_2, t_p is the carrier period. The target of NP potential balancing algorithm is to generate the reference average NP current $i_{NP,ref}$ and then regulate the NP potential to its normal value.

5.2. Relationship between the average NP current and zero-sequence voltage

As the only freedom degree in the carrier-based PWM zero-sequence voltage does not influence the output line voltage and current. It leads to different pulse patterns and so results to different NP currents. However, the relationship between average NP current and zero-sequence voltage in the 5L-ANPC inverter is very complex. If a zero-sequence voltage uz is injected into the three-phase reference voltages, the actual reference voltages can be written as follows:

$$u`_x = u_x + u_x \quad (5)$$

The injection of zero-sequence voltage changes the reference phase voltages and then affects the NP current. Not only that, the selection of redundant switching states also affects the NP current. In the practical control system, to maintain the floating capacitor voltage balanced, which redundant switching state is used is determined by the floating capacitor voltage and current polarity. It must be calculated according to the actual reference voltage $u`_x$ and the switching state currently selected. The average NP current of three phases in a carrier period can be obtained as:

$$\bar{\imath}_{NP} = \bar{\imath}_{NPa} + \bar{\imath}_{NPb} + \bar{\imath}_{NPc} \quad (6)$$

5.3. NP Potential Balancing Method

Since the relationship between the NP current and zero-sequence voltage is not linear and continuous, it is still hard to compute the precise zero-sequence voltage to generate the reference NP current directly. A simple solution to this problem is to select a limited number of zero-sequence voltages which are called key zero-sequence voltages. Calculating the corresponding average NP currents of these key zero-sequence voltages and comparing them with the demanded average NP current , the one who generates the most approximate NP current is chosen as the most appropriate zero-sequence voltage.

In order to reduce the computation time and switching losses, the zero-sequence voltages who make at least one of the three reference phase voltages an integer (–2, –1, 0, 1, or 2) are chosen as the key zero-sequence voltages. Then at least one of the three phases switches will stay still during each carrier period, which can be regarded as an equivalence of five-segment space vector PWM (SVPWM). Defining the minimal, medium and maximal values of u_a, u_b and u_c are u_{min}, u_{mid} and u_{max}, respectively, in order to avoid over modulation, the span of the zero-sequence voltage can be injected is expressed as:

$$u_{zmin} \le u_x \le u_{zmax} \quad (7)$$

where

$$u_{zmin} = -2 - u_{min}\ ,\ u_{zmax} = 2 - 2\ u_{max} \quad (8)$$

are defined as the minimal and maximal zero-sequence voltages that can be injected, respectively.

6. SIMULATION RESULTS AND ANALYSIS

To verify the above design and analysis, a simulation model was developed in Mat lab\Simulink. In the simulation, load is set at 15 kW. The load will be activated at 0.02s. The STATCOM can be connected or disconnected from the grid with the help of a manual switch. The values of current, voltage can be varied with the connection of the STATCOM.

The respective Simulink output waveforms for the given model are shown in figures 3 to 6.The total harmonic distortion was analysed for the source current. Initially the load is not connected to the system. With the connection of the load with the circuit after 0.02 s the change in current and the voltage values are noted. The Figure 3 shows DC link capacitor voltage waveform. The voltage of the DC link capacitors are maintained according to the operation of the converter. After the operation of the STATCOM the voltage is balanced and maintained constant.

Table-3: Three Phase Source Block

PARAMETERS	VALUE
Phase to phase RMS voltage (V)	400
Phase angle (degrees)	0
Frequency (Hz)	50

Table-4: Three Phase Load Block

PARAMETERS	VALUE
Nominal Phase to phase RMS voltage (V)	400
Nominal Active Power (W)	$15e^{03}$
Nominal Frequency (Hz)	50

The waveform for the source current is shown in Fig 4. The load is connected to the source at the time of 0.02 sec. After that the source current magnitude gets changed and the deviation of the magnitude is compensated by the compensation current. The specifications of source and load blocks are given in the Table 3 and Table 4.

The Total Harmonic Distortion was determined with FFT analysis and the window is shown in Figure 5 and Figure 6. The total harmonic distortion was analyzed for the source current. The IEEE standard for the THD is below 5%. The obtained THD level is 4.91%.

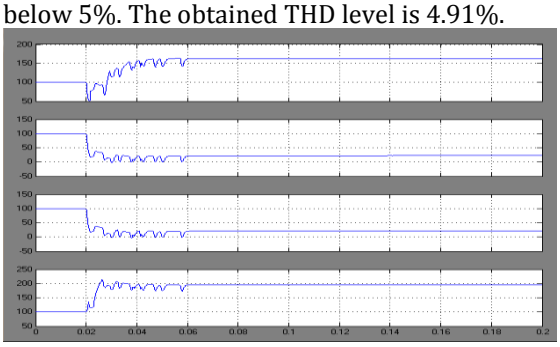

Fig-3: Voltage waveform across the capacitor

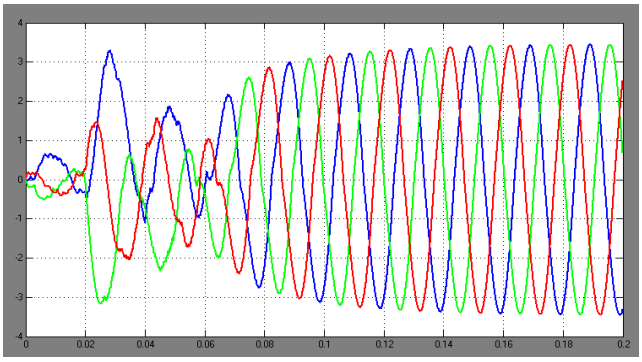

Fig-4: Waveform of the source current

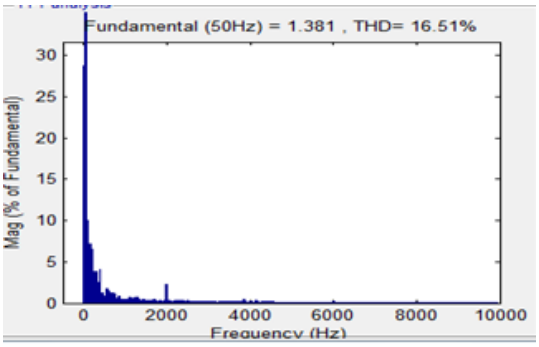

Fig-5: THD analysis of source current before connecting to STATCOM

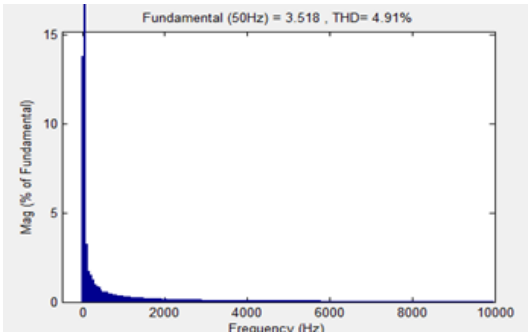

Fig-6: THD analysis of source current after connecting to STATCOM

7. CONCLUSION

This paper presents the PDPWM technique with DC-link capacitor voltage balancing control for active neutral point clamped converter based STATCOM. The voltage balancing of dc-link capacitors is achieved by zero-sequence voltage injection. The relationship between the average NP current and the zero-sequence voltage is discussed, and it can be concluded that the average NP current is linearly proportional to the zero sequence voltage. So, an optimum zero sequence voltage can be calculated to regulate the dc-link capacitor voltages.The voltages on the DC link capacitors are well balanced with very small ripple. The system has low harmonics in the input current. The total harmonic distortion (THD) of input current was low with fundamental frequency switching. Simulation results conclude that the proposed PDPWM strategy is able to carry out the voltage-balancing task, with no requirement for additional power circuitry. The source current harmonics is reduced to a considerable level. The maximum allowable Total Harmonic Distortion level as per IEEE standard is given as 5%. Here, the Total Harmonic Distortion level of the source current is reduced upto4.91%.

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