GRAPHENE BASED TUNNEL FET

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Abstract -*In this paper, Graphene Based Tunnel Field Effect Transistor is presented. Graphene based tunnel field effect transistor mainly based on quantum tunneling from a graphene electrode through a thin insulating barrier. Graphenes are mainly used for grow film on substrate having much lower thermal coefficient. For preparing this hexagonal boron nitrite are used with oxidized Si wafer (300 nm of SiO_2) and DRY transfer procedure are used to obtain monolayer graphene on to hbN crystal (20-25 nm thick) and this graphene layer reports for Dirac point . For tunneling of the device considered 1 to 30 hbN layers and doping concentration for encapsulated graphenes are approximately 0 and 10^{11} that describes current-voltage characteristics over a wide range of operating conditions and provides viable route for high speed graphene tunnel field effect transistor with higher stability. The lack of an OFF state has been the main obstacle to the application of graphene based transistors in digital circuits. Recently vertical graphene tunnel field effect transistors with a low OFF state current have been reported; however, they exhibited a relatively weak effect of gate voltage on channel conductivity.*

Key Words:Graphene,Tunnel Field Effect Transistor,Gate Voltage

1.Introduction

Graphene is highly transmittance material around 97.7% with high current density(10^8amp /cm^2) This material is most stronger than steel having 1100 GPa modulus and have atwo dimension honey combed structure of allotrope Carbon.Bare graphene is a semimetal with a zero band gap and shows performance of sp^2 hybridized material as shown in fig-1.
A graphene based tunnel FET possess unique high frequency properties due to their high carrier mobility. Application of these FETs in digital circuits is, however, impossible due to the low ratio of ON to OFF state currents[1-4].

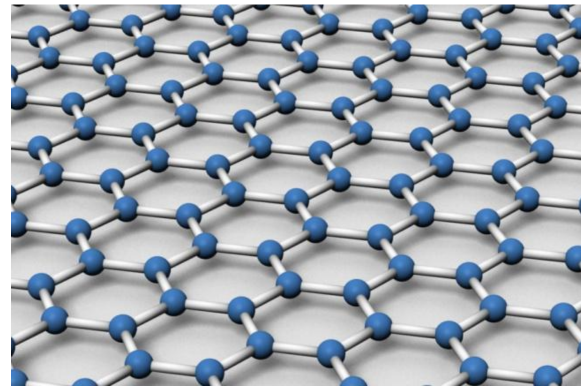

Fig -1: Graphene structure

The vertical construction represented two parallel graphene sheets (source and drain) separated by a thin tunnel transparent dielectric layer of boron nitride. Both the barrier height and electron density in the contacts were controlled by the bottom gate. The measured characteristics showed that the influence of the gate voltage on the channel conductivity was weak (non-exponential) and the ON/OFF ratio reached only 50.The dependence of the current on the gate voltage in the proposed device is exponential with an inverse sub threshold slope reaching $(60\ mV/dec)^{-1}$ at room temperature. Considering the current–voltage characteristics of the device we take into account simultaneously both tunnel and thermionic current and show that the inverse sub threshold slope of the proposed FET (as well as of any schottky barrier FET) is limited to $(60\ mV/dec)^{-1}$.The performance of graphene-based tunnel field effect transistors has been hampered by graphene'smetallic conductivity at the neutrality point (NP) and the unimpeded electron transport through potential barriers due to Klein tunneling, which limit the achievable ON-OFF switching ratios to $\sim10^3$ and those achieved so far at room temperature to less than 10. These low ratios are sufficient for individual high-frequency transistors and analogue electronics but they present a fundamental problemfor any realistic prospect of graphene-based integrated circuits. A possible solution is to open a band gap in graphene, for example by using bilayer graphene , nanoribbons ,quantum dots or chemical

derivatives but it has proven difficult to achieve high ON-OFF ratios without degrading graphene's electronic quality[5-6].
Here Table-1 shows some special properties[8] of graphene that are useful in fabrication of graphene based tunnel FET.

Table -1:Properties of Graphene

Parameter	Value and units	Observations
Mobility	40 000 cm ^{2}/VS	At room temperature (intrinsic mobility 200 $cm^2V^{-1}s^{-1}$ in suspended structures)
Mean free path (ballistic transport)	200- 300 nm	At room temperature
Fermi velocity	c/300=1000000 m/s	At room temperature
Thermal Conductivity	5000 W/m K	Better thermal conduct than in most crystals

2.Methodology

The development of GFET devices has been accompanied by the appearance of electrical models that can be used to describe the electrical characteristics of the device. For convenience of characterization, both source and drain electrodes were made from graphene layers in the multi terminal Hall bar geometry. This allows us to measure not only the tunnel current-voltage curves (I-V) but also the behavior of the graphene electrodes, thus providing additional information about the transistor operation[7].
To fabricate the device shown in Fig -2 we first prepared relatively thick hBN crystals on top of an oxidized Si wafer (300 nm of SiO2). Graphenewas then transferred onto a selected hBN crystal (20 to 50 nm thick) using a dry transfer procedure. After deposition of metal contacts (5nmTi/50nm Au) and etching to form a multi terminal Hall bar mesa, the structure was annealed at 350°C in hydrogen-argon atmosphere. In this structure this hBN layer served as the tunnel barrier[8].

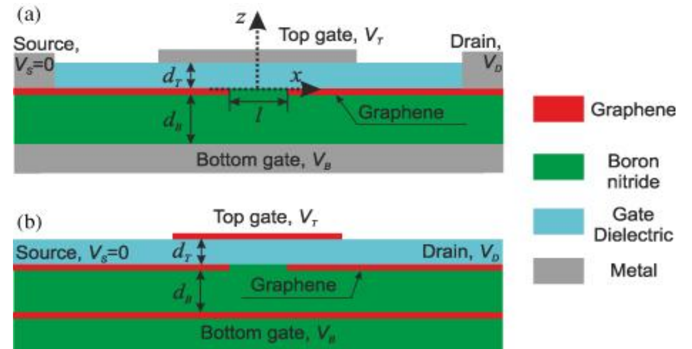

Fig-2: Schematic view of the proposed GTFET structures(a) tunnel contact in the middle of the channel (b) tunnel contact near the drain.

2.1 Tunnel Field Effect Transistors withgraphenechannels

Assuming that the Fermi level in graphene at the source and drain contacts is located exactly between the conduction and valence bands (at the so called Dirac point), one can directly obtain the electron and hole concentrations in the channel. As $e\Phi_0$ is the local Fermi energy, at low temperatures (kT<<$e\Phi_0$) and a positive gate potential one arrives at a simple expression for the electron concentration
$Ne = e^2\Phi_0^2/\pi h^2 vF^2$
The potential in the tunnel contact, determining the height of the barrier for tunneling electrons, significantly depends on the ratio L/d in structures with a barrier in the middle of the channel. It is reasonable to assume that for long barriers (L >>d) the potential inside the barrier equals V_G almost everywhere except near the graphene edges. At L<<d, on the contrary, the gate potential almost does not penetrate into thetunneling gap. In this case the barrier height counted off from the Dirac point does not depend on the gate voltage; the latter just controls the charge carrier concentration in grapheme, here the gate voltage barely affects the barrier height.
In the following we considered two characteristic potential profiles along the FET channel. The first one corresponds to a long tunnel gap in the middle of channel the corresponding band diagram is shown in Fig-2. The second type of potential distribution corresponds to a FET with a tunnel contact outside the gated section, the corresponding band diagram is presented in Fig. 3. We also assumed that the applied source–drain voltage drops only at the tunnel contact but this assumption is valid if the resistance of the tunnel contact markedly exceeds the resistance of the graphene sheet. In both situations (Figs. 2

and 3) the tunnel barrier will be treated as trapezoidal in form[9-10].

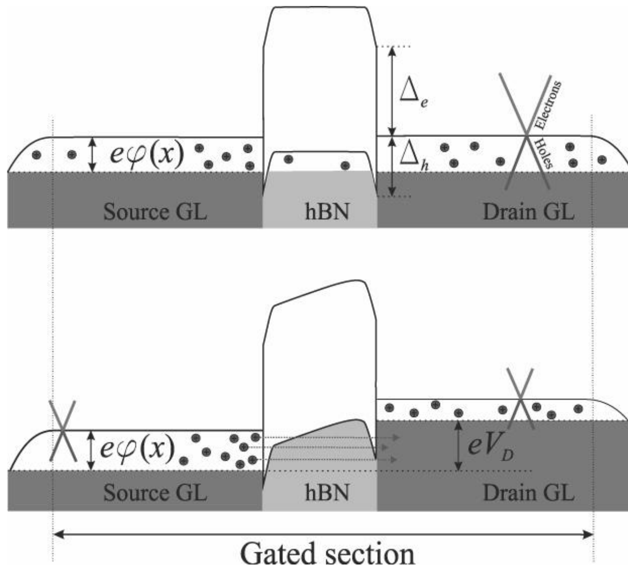

Fig.-3.1:.Band diagrams for a graphene FET with a tunnel contact in the middle of the channel ($L >> d$) at zero drain voltage (from the top) and positive drain voltage V_D.A cross indicates the position of the Dirac point withrespect to the band diagram.

Fig-3.2: Band diagrams for a grapheneFET with a tunnelcontact near the drain at zero drain voltage (from the top)and positive drain voltage V_D. A cross indicates the position of the dirac point with respect to the band diagram.

2.2.Simulation methodology and characteristics

MATLAB software is used for simulation of graphene based tunnel field effect transistor. The simulator allows ready definition of a wide variety of complex device material and their properties[11-13].The characteristics of a graphene tunnel FET with a short tunnel gap near the drain exhibit a completely different behavior, At Vgclose to zero, corresponding to tunneling from states close to the NP, the tunneling DOS in both graphene layers is small and non-zero, due to residual doping, disorder and temperature. In fig-4 I_D - V_G curve is obtained using MATLAB software. This curve explains qualitatively the main features in the measured data in GTFET.

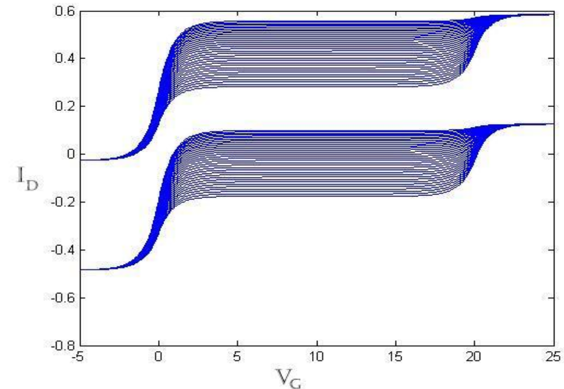

Fig-4: Current vs. gate voltage for a graphenebased tunnel FET with a tunnel contact near the drain.

3.Result and Discussion

In this paper we have tried to analyze the fabrication process of GTFET and I-V characteristics of graphene based TFET.The characteristics of a graphene tunnel FET with a short tunnel gap near the drain exhibit a completely different behavior that a power law dependence of the current on gate voltage was observed when the gate affected only the density of states of tunneling electrons but not the barrier height .As it was discussed earlier that it is accurate enough to capture the electrical characteristics of the devices .The simulated and modeled drain currents of the device shows that the value of the thickness of the top-gate oxide does not affect the accuracy of the model neither does the value of the thickness of the bottom-gate oxide. It provides a perfect platform to explore the unique electronic property in two dimension .It can be embedded in circuit simulation tools. .

Here two tables are shown below, table-2 forDrain Current and gate voltage for a graphene tunnel FET with a tunnel contact near the drain for different constant values of drain voltage, gap length is L =1 nm, gate dielectric thickness is d = 5 nm, temperature is T = 300 K.

Table-2:

Drain Voltage (V_D) (Volt)	Gate Voltage (V_G) (Volt)			Drain Current (I_D) (mA)		
0.4	1	2	3	0.1	0.4	1.0
0.2	1	2	3	0.05	0.2	0.4
0.1	1	2	3	0.01	0.03	0.2

Table-2 for Gate Current and Drain voltage for a graphene tunnel FET with a tunnel contact near the drain for different constant values of Gate Voltage .gap length is L =1 nm, gate dielectric thickness is d = 5 nm, temperature is T= 300 K.

Table-3:

Gate Voltage (V_G) (Volt)	Drain Voltage (V_D) (Volt)			Gate Current (I_D) (mA)		
2	0.2	0.4	0.6	0.2	0.4	0.7
1	0.2	0.4	0.6	0.05	0.1	0.3
0.5	0.2	0.4	0.6	0.01	0.03	0.1

From above both of the table we got the results that- Table-2, if we increases the value of gate voltage then drain current will increase for a constant value of drain voltage .Table-3, if we increase the value of drain voltage then gate current will increase for a constant value of gate voltage. Fig-4 shows that for value of gate voltage from 4 - 20 shows no change in drain voltage means it is constant or shows saturation region .if we are comparing graphene tunnel FET characteristics with characteristics of graphene FET we got the result that there is no saturation region for graphene FET means graphene TFET shows high stability performance comparatively to GFET.

4.Conclusion

The graphene is extremely well-suited for high performance tunnel transistors. The grapheneTFET derives its benefit from the material's properties and the tunneling mechanism, and can simultaneously achieve a high speed and low power dissipation. Device shows largest achievable current in the on state (I_{on}) as well as the smallest current when the device is switched off (I_{off}) and shows high stability with lower dynamic power. The limitation of this device isthe value offitting parameters should be changed from device to device.

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