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A REVIEW ON BIT ERROR RATE PERFORMANCE MEASUREMENT FOR WIRELESS SYSTEM USING VHDL

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Abstract -*Bit Error Rate Tester(BERT) is a procedure or device that measure the bit rate of transmitted signal to determine whether error were introduced into system when data was transmitted. The number of bit errors were divided by the total number of bits transferred. The propose BER tester (BERT) integrates baseband signal processing each modules of communication system along with a realistic fading channel simulator and an accurate Gaussian noise generator on to FPGA to provide an repeatable test environment. The FPGA-based BERT should reduced the time needed for simulations , which increased the productivity. The BERT modules were developed using device independent HDL. Therefore, the system became portable and easily synthesized .FPGA solutions provide cost reduction as compared to other commercially available solutions. Here we were using XILINX and simulator.*

Key Words **:BIT ERROR RATE TESTER (BERT), FIELD PROGRAMABLE GATE ARRAY (FPGA), FADING CHANNEL SIMULATION , GUASSION NOISEGENERATOR (GNG).**

1. INTRODUCTION

The wireless system developed using the modern communication techniques were largely affected by the design productivity. It is critical at the earlier stage of design to verify the design characteristics to minimize costly design issues. The bit error rate (BER) performance metric is widely used to measure the reliability of the communication systems. Monte Carlo (MC) simulation techniques had been widely used to generate BER versus a range of expected signal-to-noise ratio (SNR) conditions. However, execution time of software-based MC simulations were very long which increased complexity of system. BERT used to quantify a channel carrying data by counting the rate of error in data string. It is used in telecommunication , network and radio communication system. It is key parameter that s used in accessing system that transmit digital data from one location to another. It is used for radio link & fibre optic communication system or any system that transmit data over a network where noise, interference may cause loss of digital signal. Although there are some differences in the way system work but basic were same. When data transmit over a data link there were a possibility of error being added. If error occur in the data then efficiency of system reduced.. As a result it is necessary for system to access the performance & BER. BER provide ideal way in which this can be achieved. BER access end to end performance of system consist of transmitter & receiver & medium used. In this way BER enable actual performance of system can be tested. If the medium between them was good then SNR was high and BER was very small . The main reason for degradation of a data channel and corresponding BER. Both effect have random element to them the noise following guassian probability function while the propagation model followed Rayleigh model hence we can said characteristic are normally undertaken using satisfied analysis technique. To find out the BER performance using MC simulation method, we have to measure the BER on large number of independent problem instances .Under additive white Gaussian noise (AWGN) channels system performance simulation of digital communication systems were averaged over a large number of independent instances of data and noise. Hardware-based baseband BER measurement systems uses field-programmable gate arrays (FPGAs) and use model-based systems such as Simulink to integrate parameterizable IP blocks on FPGA. Using system level tools were eliminate the time needed for hardware knowledge and were shorten the design time, a simulation library may include only a set of basic components and might not include modules, such as new coding algorithms for emerging technologies.

2. PROPOSED WORK

To demonstrate our methodology, we will parameterizable software-based baseband BERT for multiple antenna communication systems.The block diagram of the proposed communication system is as given in diagram 1.The

implementation has been done using VHDL in Xilinx ISE 12.2 and simulated using simulink . Channel coding is applied to the data bits to improve system performance and robustness in the presence of channel impairments. Typically, the fading channel response changes much slower than the data signal. Therefore, the effects of a deep fade can last over a relatively long sequence of data samples, which can result in a burst of errors. Interleaving the data samples before transmission causes bursts of errors arising in the channel to be broken up by the de-interleaver in the receiver. The resulting isolated bit errors can then be more readily detected and corrected by the error correction decoder. The block diagram of the proposed communication system consist of following blocks:

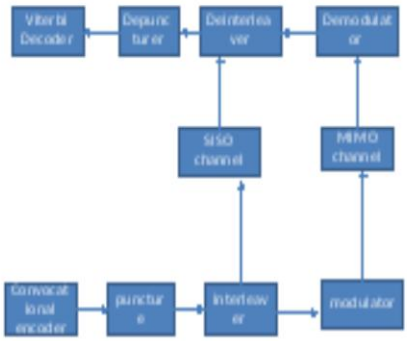

Fig 1. Block diagram of the proposed communication system

2.1 Convolutional Encoder: The source bit data is given to the input of the encoder. It encode the sequence of binary input vector to produced a sequence of binary output vectors. This block performed operation of forward error correction.

2.2 Puncturer: The output of encoder is given to the puncture, where some of the output parity bits of the encoder are deleted as per the puncturing matrix. This has the same effect as encoding with an error correction code with a higher rate, or less redundancy.

2.3 Interleaver: The output of puncturer is given to an interleaver which correct the burst errors from the output. The interleaver concept is Implemented using two temporary 50 bit registers and counters. The data is written sequentially into the locations .

2.4 Modulator: The output of the inter leaver is appended with a zero to make it 4 bits, which is then mapped to signal constellation using the 16 QAM modulation techniques.

2.5Demodulator: The received signal through the channel is demodulated using the reverse process in demodulator, where the 4 bit data is recovered.

2.6 Deinterleaver: Here the opposite operation of the interleaver takes place.

2.7 De puncturing: The same puncturing matrix is used at the receiver side which introduces dummy bits.

2.8 Viterbi decoder: The output of the de puncturer is fed to Viterbi decoder. It uses viterbi decoding algorithm for decoding a bit sequence that has been encoded using forward error correction technique based on convolution code. It consist of three different parts. They are the path metric unit (PMU) which consist Add Compare Select (ACS), the branch metric unit (BMU) and the survivor memory management unit.

2.8.1 Branch metric unit :

Here hamming distance computation is done. It compares the received data with the expected output of the encoder .

2.8.2 Add compare & select unit :

The path metric unit calculates the path metric by adding the path metric of received symbols with the path metrics of the previous stage.

2.8.3 Survivor memory management :

This unit used for storing the survivor path values..

2.8.4 Trace back unit :

Here the survivor path and the output data are identified.

3. CONCLUSIONS

In this paper, the idea of using Xilinx was proposed to measure the bit error rate using software. Compared with traditional standalone BERT & ATE equipment it is cheaper. FPGA Based solution provide testing under different noise condition.

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