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Design and analysis of SRAM cell for ULP application

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Abstract-*The rapid advancement in processors, controllers, digital system and portable electronic system demands ultra low power consumption. The above devices consist almost 2/3rd of VLSI circuits as SRAM (Static Random Access Memory), leads majority of power consumption into the ciruit.Now there is necessity to focus on SRAM to minimize the power consumption. This paper focuses on the power dissipation during the write, read and hold operation in 4T, 5T, 6T, 7T, 8T and 9T CMOS SRAM cells. These SRAM circuits are drawn simulated on Tanner EDA Tool 13.0[11] at different technologies (16nm, 22nm and 32nm) varying the supply voltage VDD from 0.6V-1.3V[1].The average power consumption and Signal to Noise Margin (SNM)[2] of different SRAM cells are compared in different modes of operation at different technologies The results are compared among 4T, 5T, 6T,7T, 8T and 9T SRAM cell which are also being characterized in this thesis with the same technology.SNM(signal noise margin)plays an important role in SRAM stability, the comparative chart is also characterized with write, read and hold operation.*

Keywords: **Ultra low Power, SNM,SRAM, 16nm,22nm,32nm,4T,5T,6T, 7T,8T,9T SRAM cell.**

1. INTRODUCTION

The capability of handling data in chips named as memory. Static random access memory (SRAM) holds one bit of information using bi-stable circuitry. A SRAM can be designed by NMOS and PMOS transistors in CMOS technology [3]. The transistors are scaled down which also increases leakage currents and it reduces the battery life. In order to reduce the leakage current additional transistors can be added to conventional 6T SRAM [1] to have low power consumption. It reduces these adverse effects in the basic SRAM cell performance and 4T, 5T SRAM can be used for cache memory. We will observe a couple of SRAM Cells that allow the analysis and simulations of the power dissipation and signal to noise margin (SNM) [2]at 32nm, 22nm and 16nm technology[5].

1.1Static Random-Access Memory (SRAM)

Static Random Access Memory exhibits data reminisce; if memory is powered data may be lost in the conventional sense. In figure 1. 4T SRAM consists four transistors (i.e. two NMOS are load transistors and others are access transistors).It allows very high resistance for pull-up resistors and is implemented by extra layer of polysilicon which consumes more power.Eventhough it is used for cache memory. In figure 2 6T SRAM consists of four transistors (M1, M2, M3and M4 behaves as two cross-coupled inverters) and remaining transistors (M5 and M6) as access transistors. This storage cell has two stable states either 0 or 1.An Access transistors provides controls to memory cell during write and read operation. There are also other types of SRAM cells use 5T, 7T, 8T, 9T or more transistors per bit.6T SRAM cell is known as conventional SRAM cell. Additions to more transistors in conventional 6T SRAM cell provides less leakage current and more stability during read and write operation.

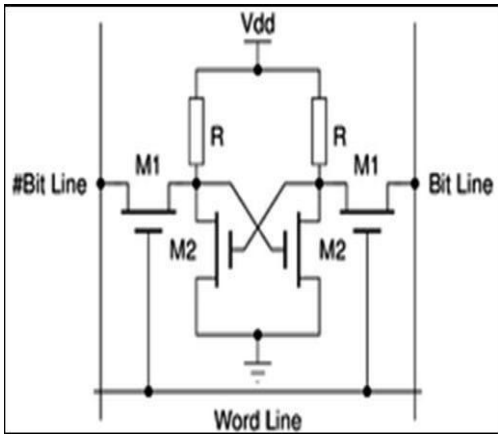

Fig. 1: 4T SRAM cell

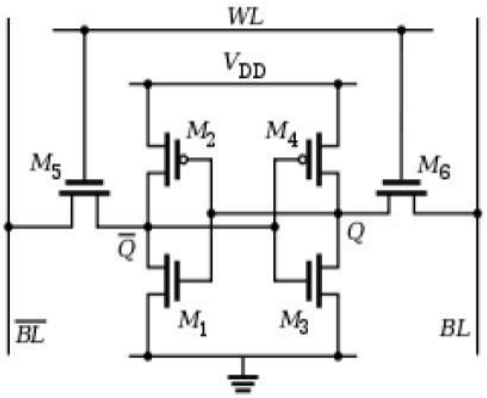

Fig. 2: 6T SRAM cell

An SRAM cell has three different states i.e. write operation (updating the contents), hold operation (the circuit is idle) and read operation (the data has been requested). The SRAM operates in read mode and write mode. The three different states of SRAM cell work as follows.

1.1.1 Hold operation

When word line voltage is kept at logic 0 the access transistors disconnect the memory cell from bit lines(BL and BLB) and two cross-coupled inverters (M1-M4 and M2-M3)continues to reinforce one another till power supply is given. These operations is assumed when there is no read and write operation of memory cell and it is also important to retain the content of memory and in power analysis of the circuit.

1.1.2 Read operation

In this operation either logic 0 or 1 to be sensed from SRAM cell through Q and QB.Assuming the content of the memory cell at Q is logic 1. Pre-charge both the bit lines (BL and BLB) to logic 1 then provide voltage to the word line WL to enable the access transistors. Now value stored at Q and QB will be transferred through BL and BLB.Since Q is at logic 1 BL will remain at logic 1 and BLB will discharge through M1 and M5. If the content of the memory is logic 0, the opposite operation will occur and BLB will charge to logic 1 and BL towards logic 0. Beside of very small voltage difference in BL and BLB sense amplifier senses whether BL or BLB have higher voltage. If sense amplifier senses higher voltage at BL then memory at logic 1 and vice versa. The sensing response of sense amplifier will decide the speed of SRAM cell.

1.1.3Write operation

The write operation starts what we supposed to write into memory. If we wish to write logic 0, we must apply voltage to bit lines (BL to logic 0 and BLB to logic 1). This is as similar as applying a reset pulse to an SR flip-flop, causes the flip flop to change the logic level. If we wish to write 1, we must invert the logic state of bit lines (BL to logic 1 and BLB to logic 0). Word line voltage (WL) is asserted to logic 1 at both the above operation. The driver transistors are kept higher (W/L ratio) than load transistors so that overriding can be done quickly in cross coupled inverters. But this may lead more power loss.

1.2 Different SRAM cells

The SRAM cell can be designed by different no of transistors in CMOS technology, which are abbreviated as 4T, 5T, 6T, 7T, 8T, 9T and many more and explained as below.

1.2.1 4T SRAM cell

Figure.3 shows 4T SRAM cell in which four transistors are used as a memory cell and pull up transistors are implemented by extra layer of polysilicon. This results high resistance pulls up transistors and finally more power consumption. Two transistors are used as access transistor. Even though it is commonly used as cache memory. It operates in different modes same as conventional 6T SRAM cell.

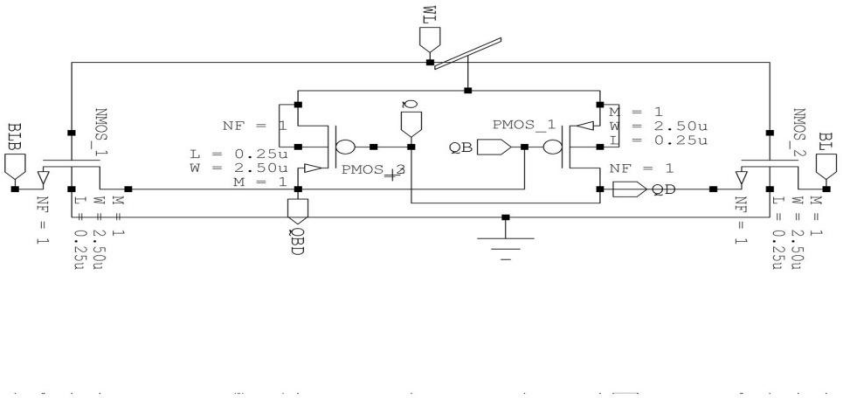

Fig. 3 4T SRAM Cell

1.2.2 5T SRAM Cell

Figure.4 is 5T SRAM cell consists of five transistors. There is only one access transistor which is accessed by bit line BL.The operation of SRAM cell is controlled by bit line voltage BL and is as similar the operation of 6T SRAM cell and quite commonly used as CPU caches in SRAM devices.

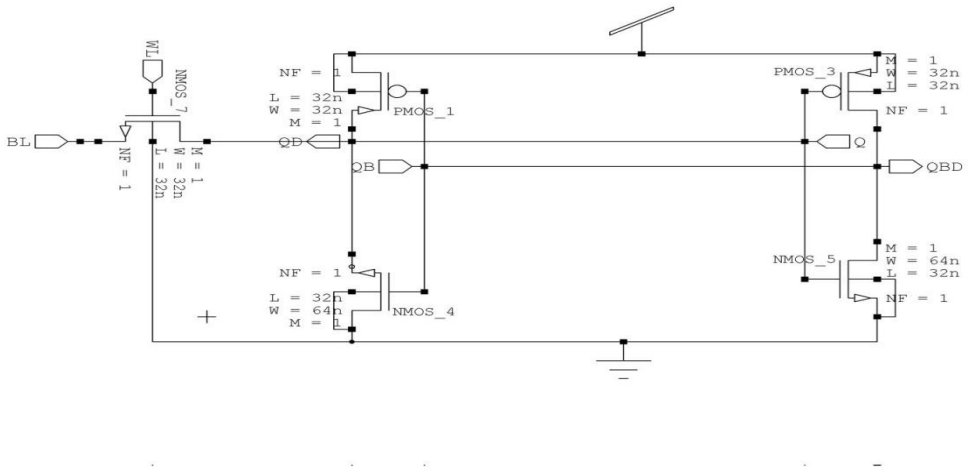

Fig. 4 5T SRAM Cell

1.2.3 6T SRAM Cell

Figure.5. shows the circuit of 6T SRAM cell [1]and consists of six transistors. The construction and working in three different modes (write, read and hold operation) of the circuit is explained above. It is conventional SRAM cell which is commonly used as memory. It operates in three different modes write, read and hold operation. These are explained as above in SRAM theory.

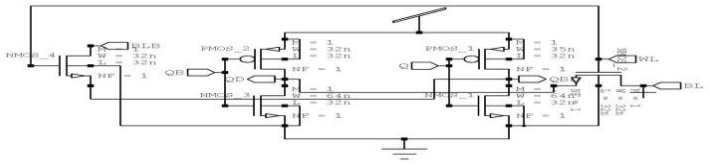

Fig. 5: 6T SRAM Cell

1.2.4 7T SRAM cell

Figure.6. shows the architecture of 7T SRAM cell. It contains of single-ended write operation and a separate read operation. In write operation cell needs either differential voltage bias or asymmetrical inverter characteristics. In another 7T SRAM cell architecture one extra transistor is used to pulls-down the cross coupled inverters. It provides stability to minimize leakage current[6]. During read operation, no differential voltage bias is provided to extra transistor to turn on which provides disturb-free operation. In 7T SRAM cell feedback between bi-stable inverters is put off in write operation. It provides very good noise margin during write operation. An extra transistor is added to the SRAM 6T cell to separate read and write operation, it gives the single-ended 7T SRAM cell.

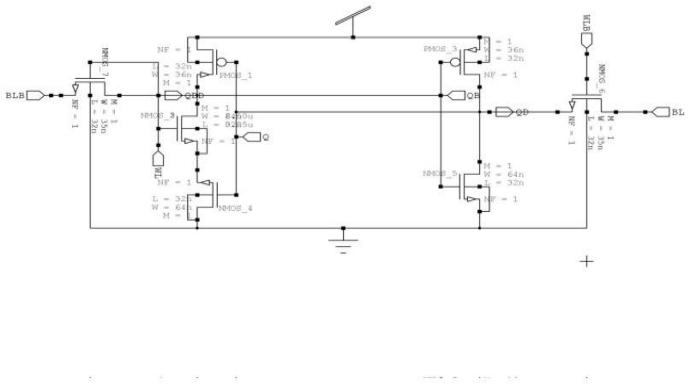

Fig. 6: 7T Cell design

1.2.5 8 T SRAM cell

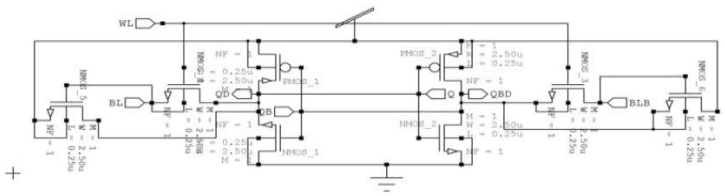

Fig.7: 8T Cell design

Figure.7. is the architecture 8T SRAM cell[7]. Two extra transistors are added as compared to 6T SRAM cell. One transistor is used to reduce gate leakage current and other transistor is used to maintain SNM of the memory cell in the zero state. Word line (WLB) signal is the complement of word line (WL) signal. Timing diagram of signal WL and WLB in different mode of operation is shown below in figure.8.The operation of 8T SRAM cell is controlled by single end sense amplifier. The operation of 8T SRAM cell can be implemented by adding additional pulse WLB in conventional 6T SRAM cell's operation.

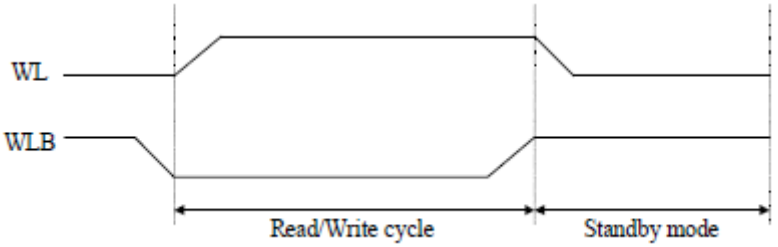

Fig. 8: Timing Diagram of 8T SRAM cell

1.2.69T SRAM cell

Figure.9. is the architecture of 9T SRAM cell[8]. It consists of 03 extra transistors with conventional cell as shown in Figure 9.The extra transistors gives complexity to the circuit but have stable SNM in read operation. It may lead to extra power consumption. One more transistor is added to 8T SRAM cell to pulls down cross coupled inverters and one more pulse voltage is required to control the leakage current [6] to the circuit. The operation of 9T SRAM cell can be implemented by adding pulse voltage (RWL and WLB) into conventional 6T SRAM cell.

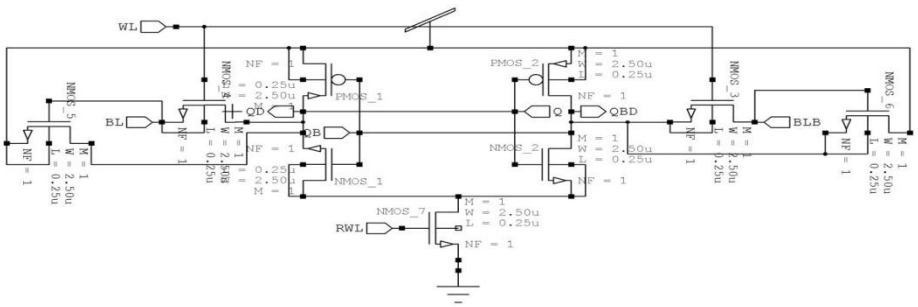

Fig. 9: 9T SRAM cell

2. Waveform of different SRAM cells after simulation at different technologies by varying supply voltage is observed

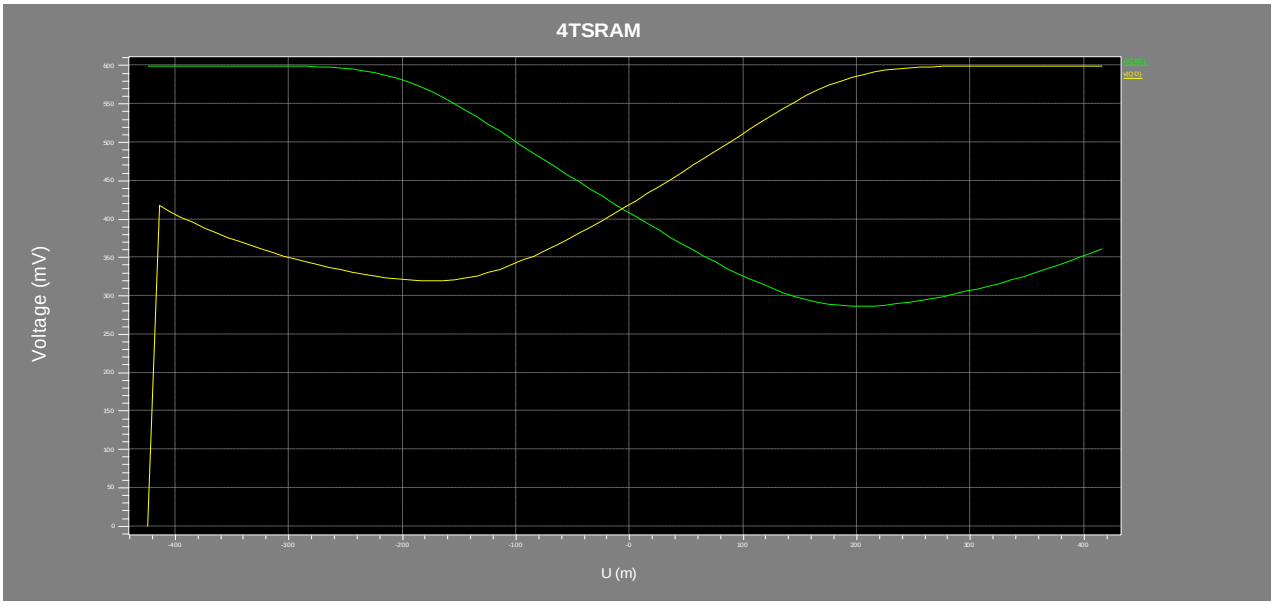

Fig. 10 4T SRAM Cell

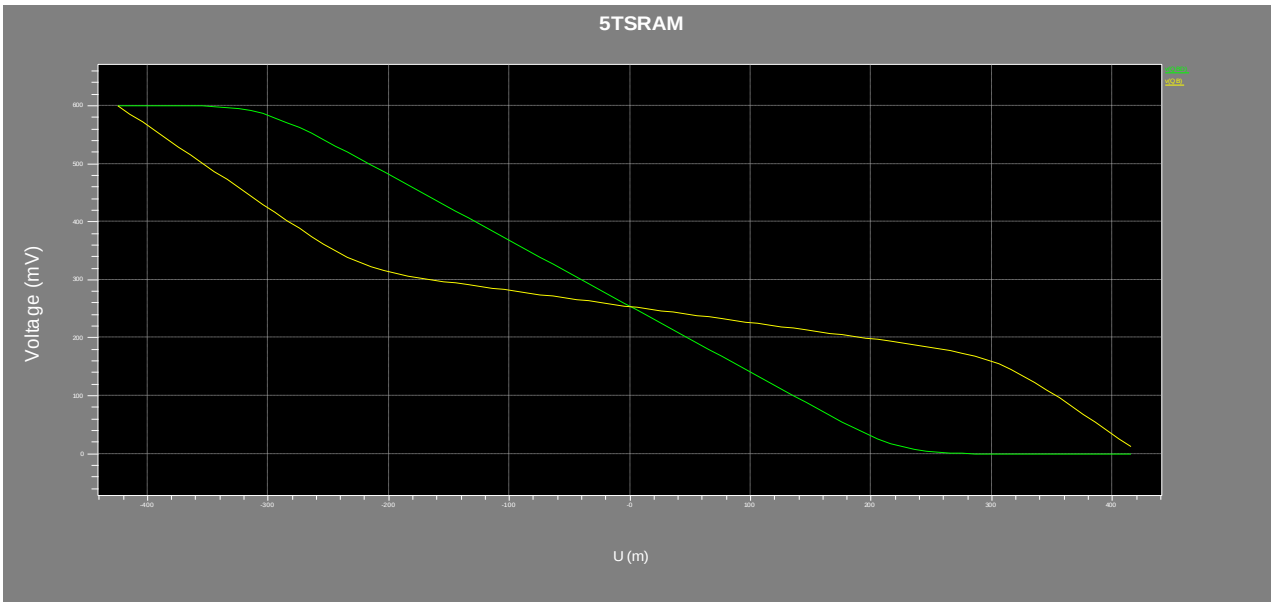

Fig. 11 5T SRAM Cell

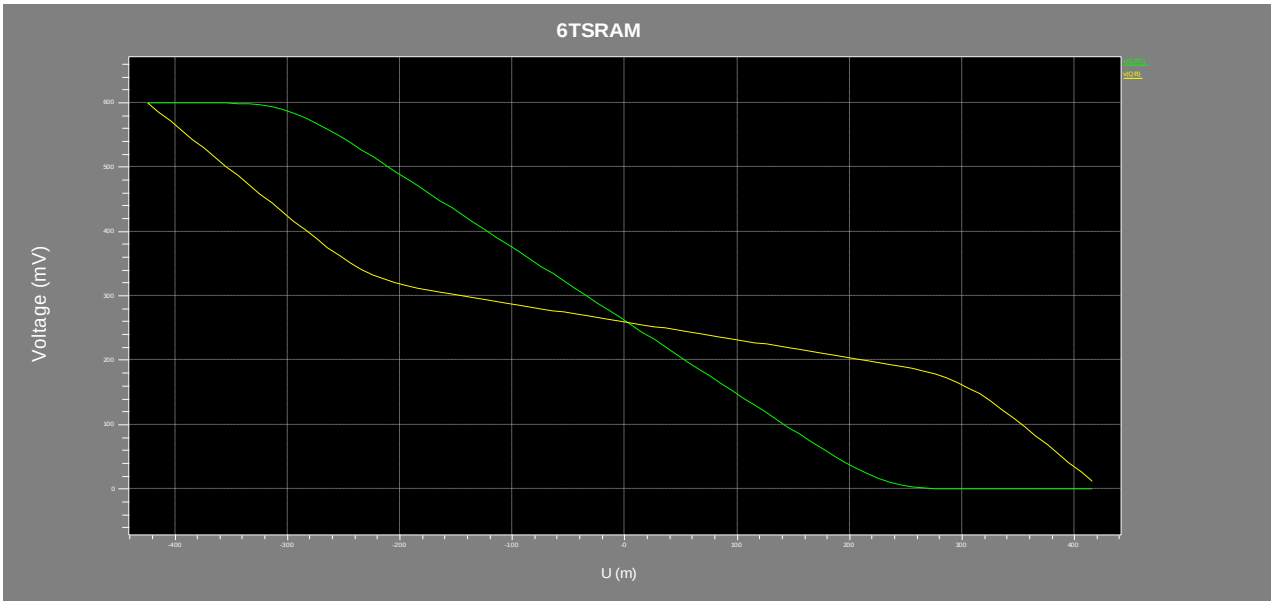

Fig. 12 6T SRAM Cell

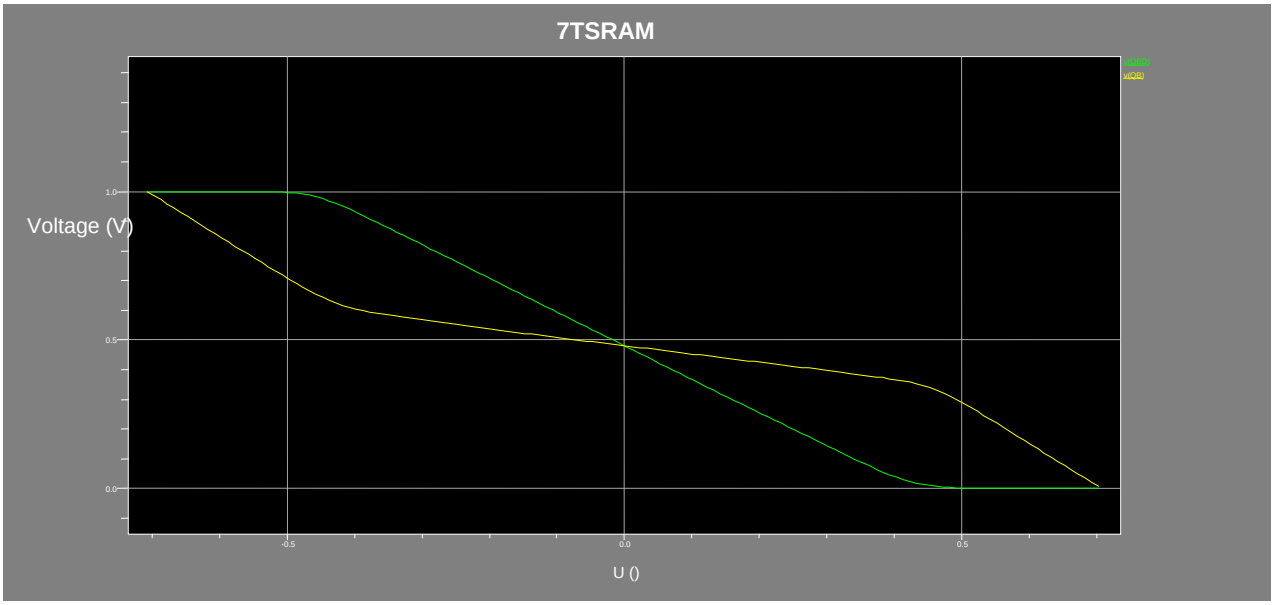

Fig. 13 7T SRAM Cell

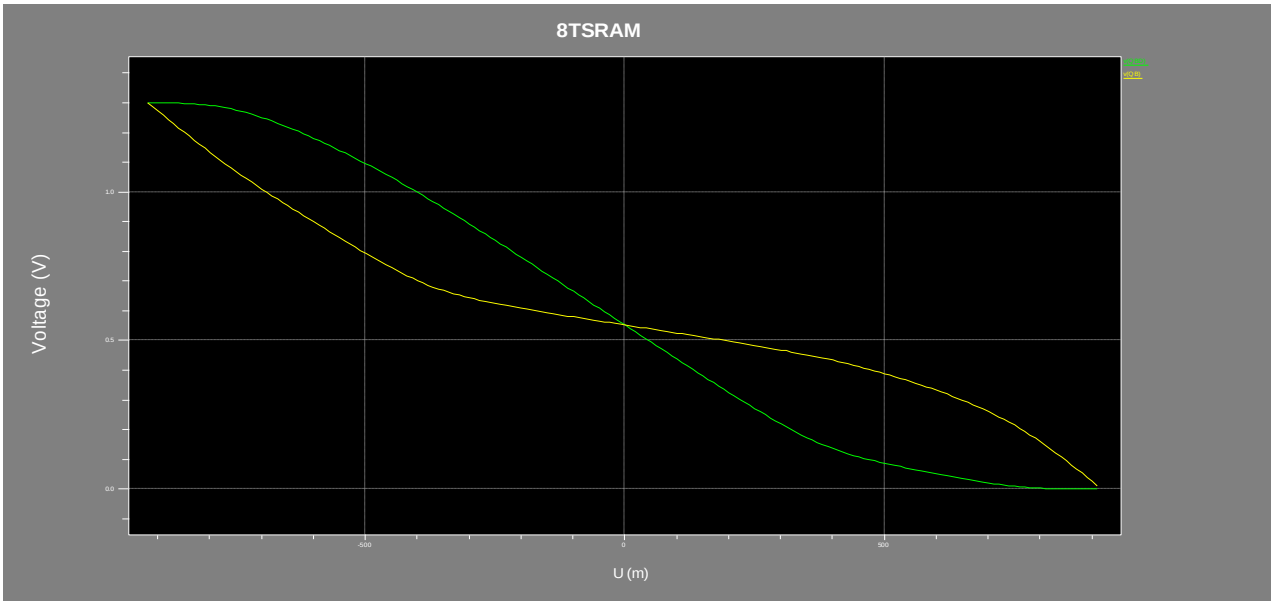

Fig. 14 8T SRAM Cell

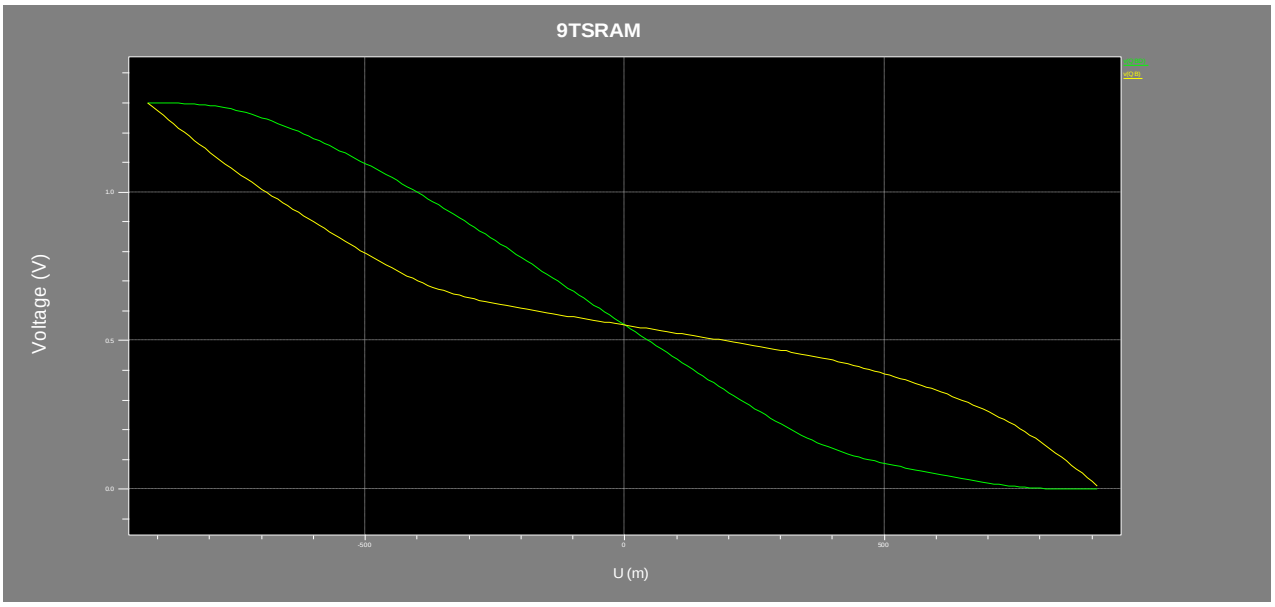

Fig. 15 9T SRAM Cell

3. CONCLUSIONS

The scaling of supply voltage has significant impact on the overall power dissipation and signal to noise margin (SNM). When supply voltage reduces, the average power and signal to noise margin (SNM) reduces quadratic ally. To achieve ultra-low-power operation[10] the supply voltage should be reduced. In this project work, we evaluated different types of SRAM bit cells suitable for ultra-low power applications. In this paper, Simulation results of 4T/5T/6T/8T/9T SRAM bit cell topologies are analyzed [11] for achieving low supply voltage and very low power operation. The following tables represent the power consumption and signal to noise margin (SNM) in different modes of operation at different technologies.

3.1Comparison of average power consumption and SNM of different SRAM cells at 16nm

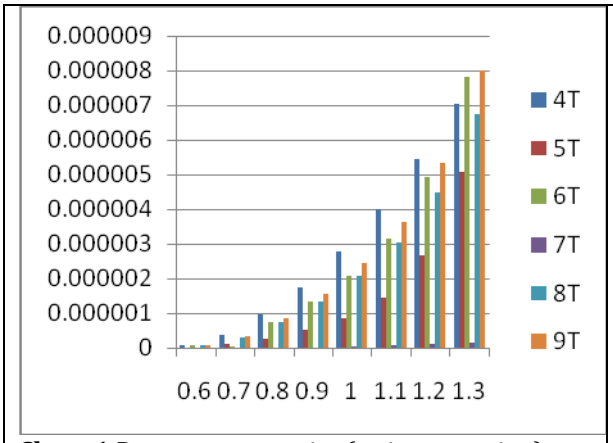

Chart-1 Power consumption(write operation)

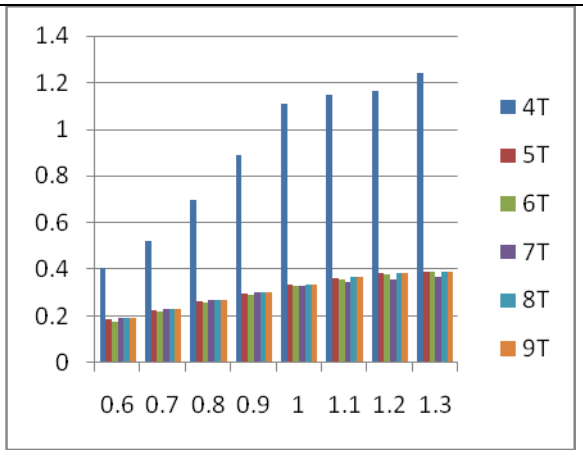

Chart-2 SNM(write operation)

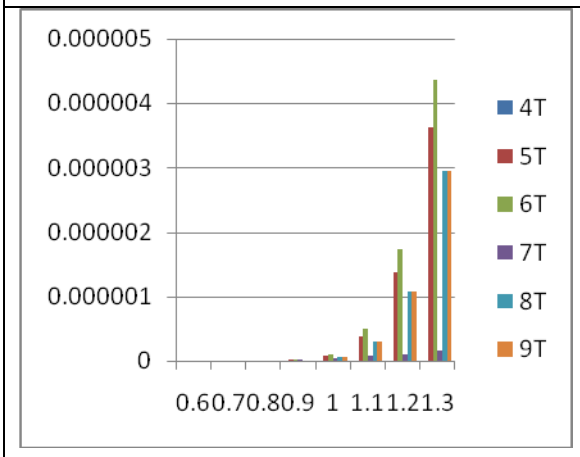

Chart-3 1 Power consumption(read operation)

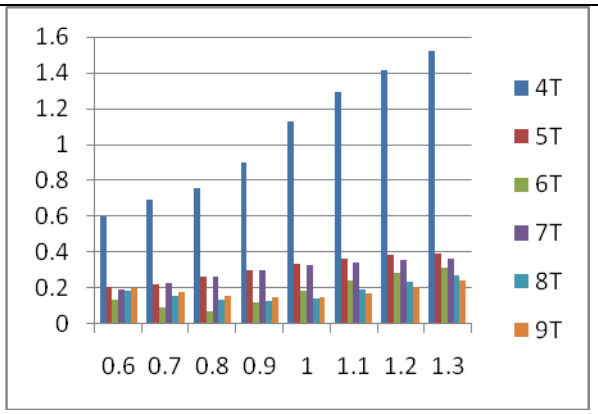

Chart-4 SNM(read operation)

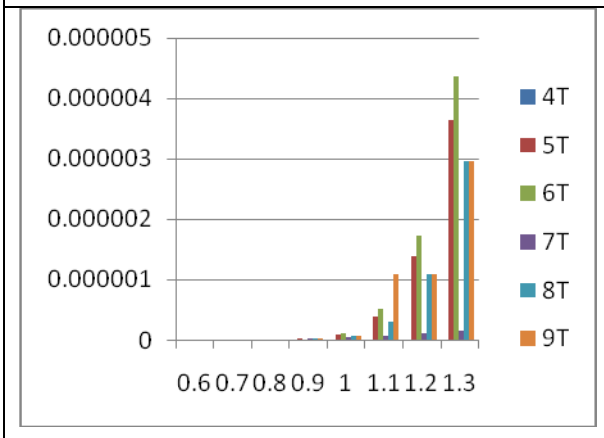

Chart-5 Power consumption(hold operation)

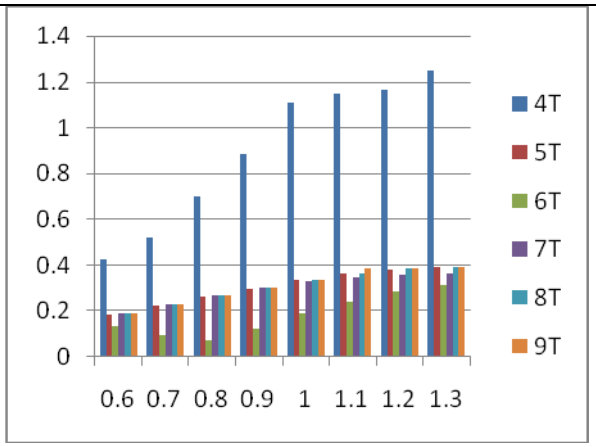

Chart-6 SNM(hold operation)

3.2Comparison of average power consumption and SNM of different SRAM cells at 22nm

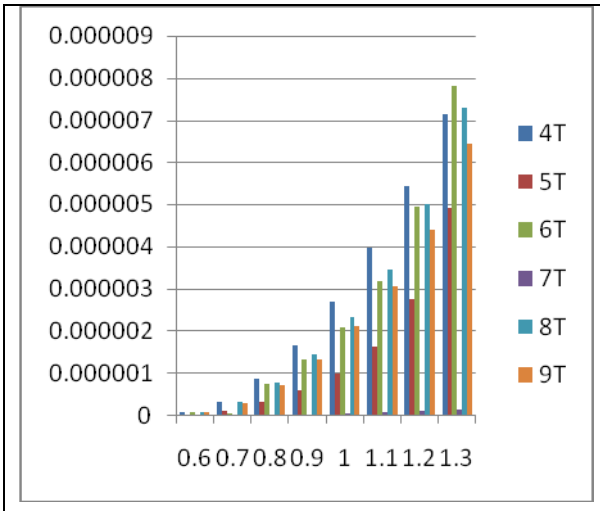

Chart-7 Power consumption(write operation)

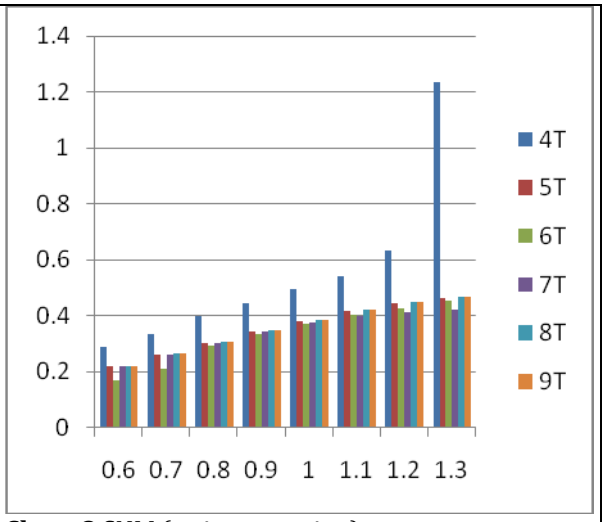

Chart-8 SNM (write operation)

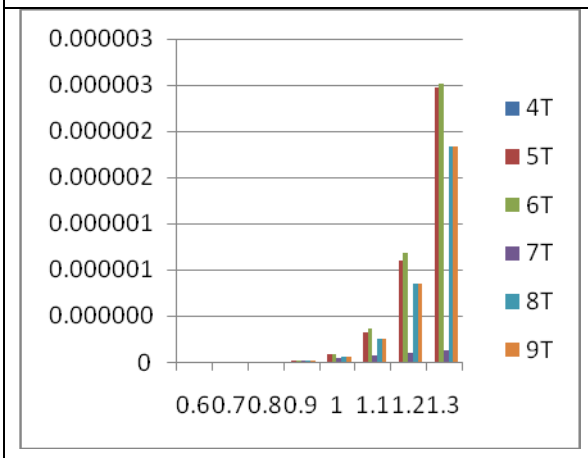

Chart-9 Power consumption(read operation)

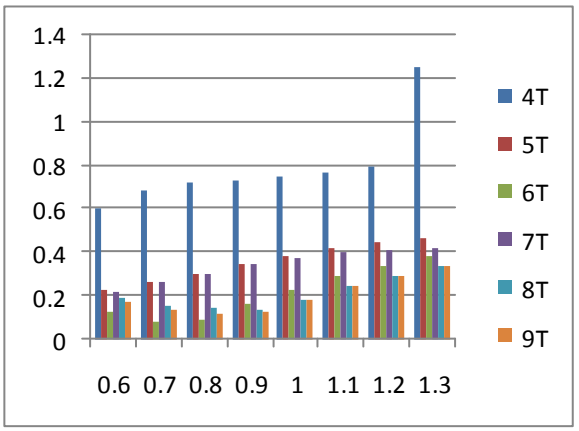

Chart-10 SNM(read operation)

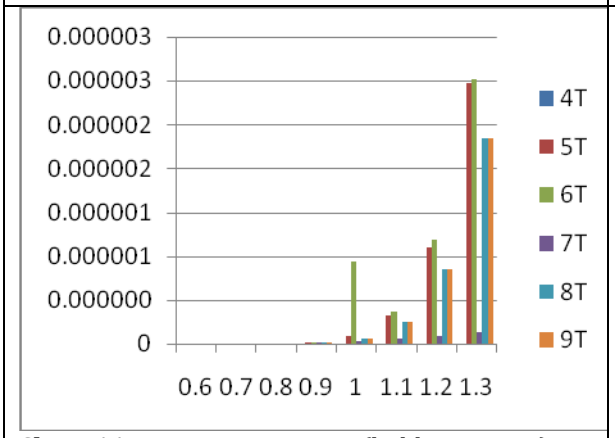

Chart-11 Power consumption(hold operation)

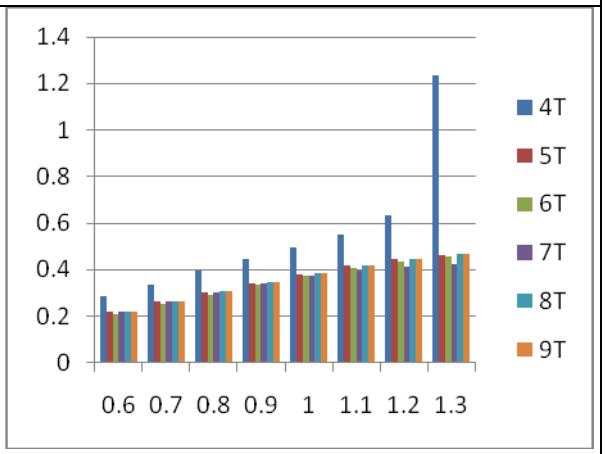

Chart-12 SNM(hold operation)

3.3Comparison of average power consumption and SNM of different SRAM cells at 32nm

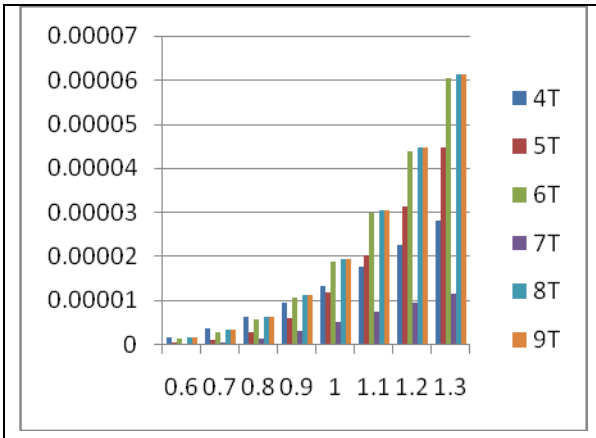

Fig. 22 Power consumption(write operation)

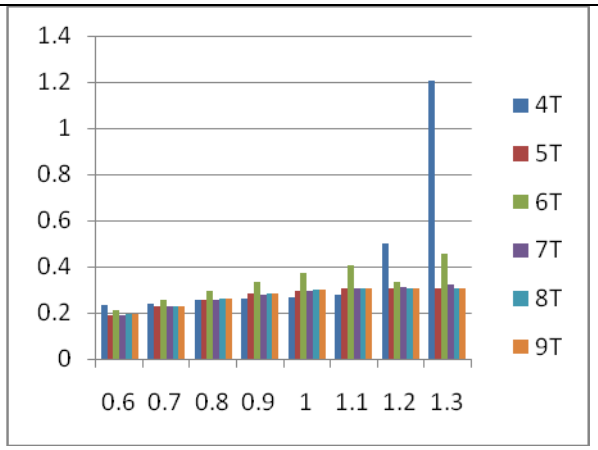

Fig. 23 SNM (write operation)

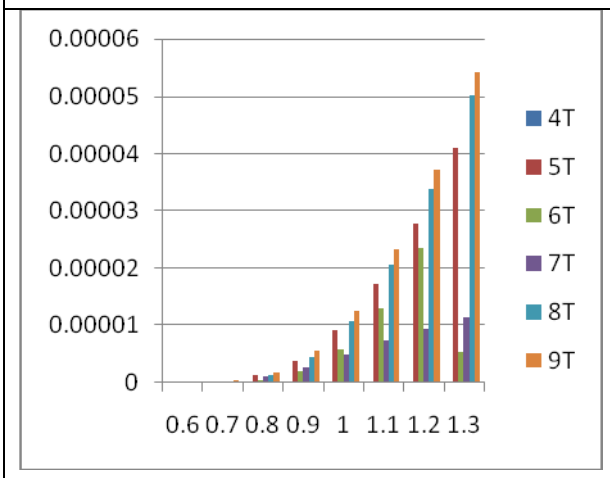

Fig. 24 Power consumption(read operation)

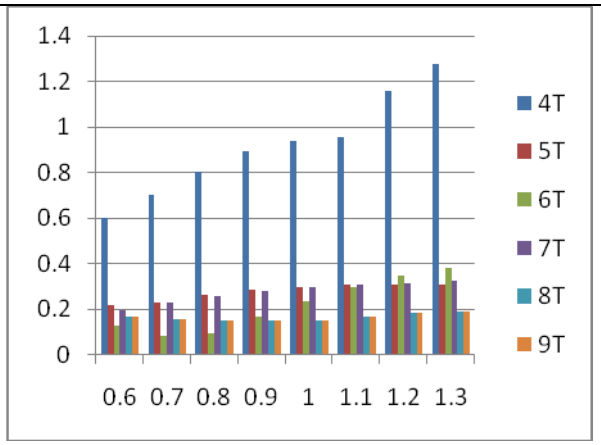

Fig. 25 SNM(read operation)

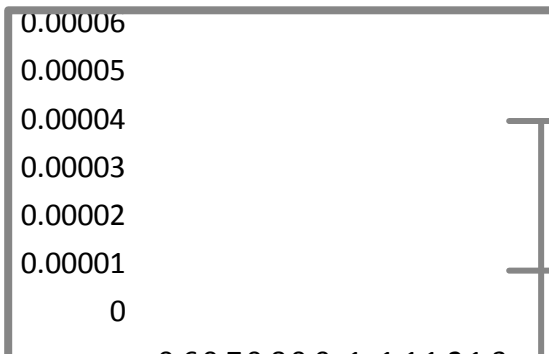

Fig. 26 Power consumption(hold operation)

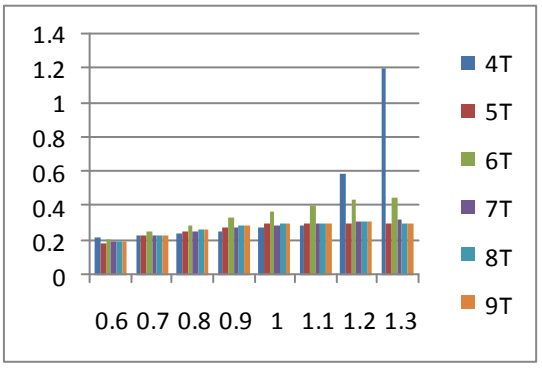

Fig. 27 SNM(hold operation)

The simulated line chart of different SRAM cells dissipates less power and more stability in compare among other SRAM cells. Despite of increasing the transistors count and area in comparison to those of other SRAM cells still dominates by total low power dissipation and supply voltage variation over this drawback. This proposed 7T SRAM cell can be used to provide low power solution and good signal to noise margin (SNM) in high speed devices at different technologies like 16nm, 22nm and 32nm.

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