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DESIGN OF HIGH THROUGHPUT ADAPTIVEFILTER USING AGING AWARE RELIABLE MULTIPLIER

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Abstract---*The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column- or row-bypassing multiplier. Digital multipliers are among the most critical arithmetic functional units. The overall performance of these systems depends on the throughput of the multiplier. Meanwhile, the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias (Vgs = −Vdd), increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed. A similar phenomenon, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Both effects degrade transistor speed, and in the long term, the system may fail due to timing violations. Therefore, it is important to design reliable high-performance multipliers. to implement the adaptive digital Least Mean Square (LMS) and delayed-LMS (DLMS) Finite Impulse Response (FIR) filtersfor typical noise cancellation applications and compare the behavior of LMS and DLMS adaptive algorithms in terms of chip area utilization and the filter critical path time or filter frequency. The direct FIR architecture is considered for filter designing and the VHDL hardware description language is used for algorithm modeling.*

Keywords--Adaptive hold logic (AHL), negative bias temperatureinstability (NBTI), positive bias temperature instability(PBTI), reliable multiplier, variable latency.

I.INTRODUCTION

Digital multipliers are among the most critical arithmetic functional units in many applications, such as the Fourier transform, discrete cosine transforms, and digital filtering. The throughput of these applications depends on multipliers, and if the multipliers are too slow, the performance of entire circuits will be reduced. Furthermore, negative bias temperature instability (NBTI) occurs when a pMOS transistor is under negative bias (*V*gs = −*V*dd). In this situation, the interaction between inversion layer holes and hydrogen-passivated Si atoms breaksis the Si–H bond generated during the oxidation process, generating H or H2 molecules. When these molecules diffuse away, interface traps are left. The accumulated interface traps between silicon and the gate oxide interface result in increased threshold voltage (*V*th), reducing the circuit switching speed. When the biased voltage is removed, the reverse reaction occurs, reducing the NBTI effect. However, the reverse reaction does not eliminate all the interface traps generated during the stress phase, and *V*th is increased in the long term. Hence, it is important to design a reliable high-performance multiplier.The corresponding effect on an nMOS transistor is positive bias temperature instability (PBTI), which occurs when an nMOS transistor is under positive bias Compared with the NBTI effect, the PBTI effect is much smaller on oxide/polygate transistors, and therefore is usually ignored. However, for high-*k*/metal-gate nMOS transistors with significant charge trapping, the PBTI effect can no longer be ignored. In fact, it has been shown that the PBTI effect is more significant than the NBTI effect on 32-nm high-*k*/metal-gate processes [2]–[4].

A traditional method to mitigate the aging effect is overdesign
[5], [6], including such things as guard-banding and gate oversizing; however, this approach can be very pessimistic and area and power inefficient. To avoid this problem, many NBTI-aware methodologies have been proposed. An NBTI-aware technology mapping technique was proposed in [7] to guarantee the performance of the circuit during its lifetime. In [8], an NBTI-aware sleep transistor was designed to reduce the aging effects on pMOS sleep-transistors, and the lifetime stability of the power-gated circuits under consideration was improved. **A**DDERS are a key building block in arithmetic and logic units (ALUs) [1] and hence increasing their speed\and reducing their power/energy consumption strongly affects the speed and power consumption of processors. There are many works on the subject of optimizing the speed and power of these units, which have been reported in [2]–[9].Obviously, it is highly desirable to achieve higher speeds atlow-power/energy consumptions, which is a challenge for the designers of general purpose processors. One of the effective techniques to lower the power consumption of digital circuits is to reduce the supply voltage due to quadratic dependence of the switching energy of the voltage. Moreover, the sub threshold current, which is the main leakage component in OFF devices, has an exponential dependence on the supply voltage level through th drain-induced barrier lowering effect [10]. Depending on the amount of the supply voltage reduction, the operation ofON devices may reside in the super threshold, near-threshold, or sub threshold regions. Working in the super threshold region provides us with lower delay and higher switching and leakage powers compared with the near/sub threshold regions. In the sub threshold region, the logic gate delay and leakage power exhibit exponential dependences on the supply and threshold voltages. Moreover, these voltages are (potentially) subject to process and environmental variations in the nanoscale technologies.

2. PREVIOUSLY PROPOSED ARCHITUCTURE

In the architecture, the column- and row-bypassing multipliers can be examined by the number of zeros in either the multiplicand or multiplicator to predict whether the operation requires one cycle or two cycles to complete[9].

When input patterns are random, the number of zeros and ones in the multiplication and multiplicand follows a normal distribution, Therefore, using the number of zeros or ones as the judging criteria results in similar outcomes.

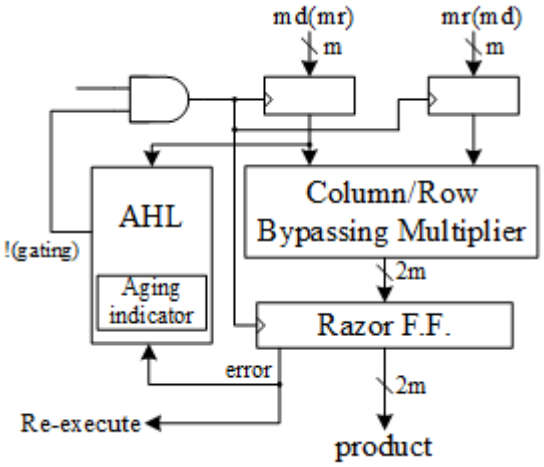

FIG.1 Aging Aware Multiplier Architecture

Aging-aware multiplier architecture, which includes two m-bit inputs (m is a positive number), one 2m-bit output, one column- or Row-bypassing multiplier, 2m 1-bit Razor flip-flops and an AHL circuit. The inputs of the row-bypassing multiplier are the symbols in the parentheses[5].

Hence, the two aging-aware multipliers can be implemented using similar architecture, and the difference between the two bypassing multipliers lies in the input signals of the Adaptive Hold Logic (AHL).

According to the bypassing selection in the column or row bypassing multiplier the input signal of the AHL in the architecture with the column by passing multiplier is the multiplicand, whereas that of the row bypassing multiplier is the multiplication. Razor flip-flops can be used to detect whether timing violations occur before the next input pattern arrives.

2.1 ADAPTIVE HOLD LOGIC (AHL)

The hold logic is holding the output at some time, because it produces delay between two functions. At the time of process any error will be occurred means AHL produces delay or hold the output few second.

When an input pattern arrives, both judging blocks will decide whether the pattern requires one cycle or two cycles to complete and pass both results to the multiplexer. The multiplexer selects one of either result based on the output of the aging indicator.

Then an OR operation is performed between the result of the multiplexer, and the .*Q* signal is used to determine the input of the D flip-flop. When the pattern requires one cycle, the output of the multiplexer is 1.

The! (Gating) signal will become 1, and the input flip flops will latch new data in the next cycle. On the other hand, when the output of the multiplexer is 0, which means the input pattern requires two cycles to complete, the OR gate will output 0 to the D flip-flop. Therefore, the! (gating) signal will be 0 to disable the clock signal of the input flip-flops in the next cycle. Note that only a cycle of the input flip-flop will be disabled because the D flip-flop will latch 1in the next cycle[7].

2.1 ARCHITECTURE PROCESS

When input patterns arrive, the column- or row-bypassing multiplier and the AHL circuit execute simultaneously. According to the number of zeros in the multiplicand (multiplicator), the AHL circuit decides if the input patterns require one or two cycles. If the input pattern requires two cycles to complete, the AHL will output 0 to disable the clock signal of the flip-flops. Otherwise, the AHL will output 1 for normal operations. When the column- or row-bypassing multiplier finishes the operation, the result will be passed to the Razor flip-flops

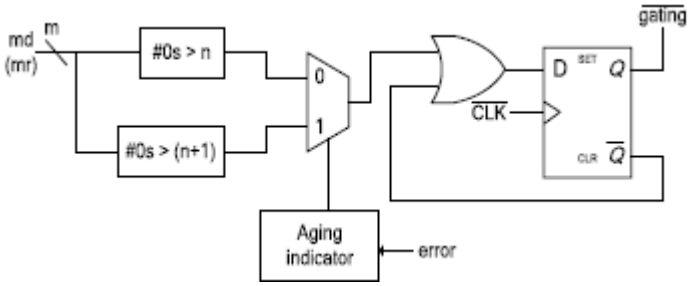

FIG.2.Agram of Adaptive Hold Logic

The Razor flip-flops check whether there is the path delay timing violation. If timing violations occur, it means the cycle period is not long enough for the current operation to complete and that the execution result of the multiplier is incorrect. Thus, the Razor flip-flops will output an error to inform the system that the current operation needs to be re-executed using two cycles to ensure the operation is correct [3].

In this situation, the extra re-execution cycles caused by timing violation incurs a penalty to overall average latency. However, our proposed AHL circuit can accurately predict whether the input patterns require one or two cycles in most cases.Only a few input patterns may cause a timing variation when the AHL circuit judges incorrectly. In this case, the extra re-execution cycles did not produce significant timing degradation.

In summary, our proposed multiplier design has three key features[6]. First, it is a variable-latency design that minimizes the timing waste of the noncritical paths. Second, it can provide reliable operations even after the aging effect occurs. The Razor flip-flops detect the timing violations and re-execute the operations using two cycles.

Finally, our architecture can adjust the percentage of one-cycle patterns to minimize performance degradation due to the aging effect. When the circuit is aged, and many errors occur, the AHL circuit uses the second judging block to decide if an input is one cycle or two cycles.

2.2. Razor Filp-Flop

The main flip-flop catches the execution result for the combination circuit using a normal clock signal, and the shadow latch catches the execution result using a delayed clock signal, which is slower than the normal clock signal.

If the latched bit of the shadow latch is different from that of the main flip-flop, this means the path delay of the current operation exceeds the cycle period, and the main flip-flop catches an incorrect result.Figure.3shows the details of Razor flip-flops. A 1-bit Razor flip-flop contains a main flip-flop, shadow latch, XOR gate, and mux [5].

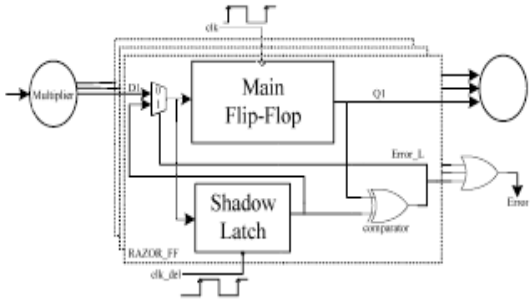

FIG.3. Diagram Of Razor Flip-Flop

If errors occur, the Razor flip-flop will set the error signal to 1 to notify the system to re-execute the operation and notify the AHL circuit that an error has occurred.

The use Razor flip-flops to detect whether an operation that is considered to be a one-cycle pattern can really finish in a cycle [8]. If not, the operation is re-executed with two cycles. Although the re-execution may seem costly, the overall cost is low because the re-execution frequency is low.

3. PROPOSED ADAPTIVE FILTER

An adaptive filter is a system with a linear filter that has a transfer function controlled by variable parameters and a means to adjust those parameters according to an optimization algorithm [4].

The direct form of an LTI FIR filter is mainly consists of shift registers, adders and multipliers.

Two different commonly used approaches provide the basis of designing FIR filters called direct and transposed architectures. The signal samples are multiplied by filter coefficients and are gathered together in the adder block [10].The transposed structure, a modification of direct form, does not consist of shift registers which makes it simpler for implementation than direct form. Two different commonly used approaches provide the basis of designing FIR filters called direct and transposed architectures.

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3.1 NOISE CANCELLATION

The basic configuration of using adaptive filters for noise cancellation applications is shown. Theperformance of adaptive filter for noise cancellation has been evaluated for three different issues used for the filter weights f0 f1, f2, and f3 are updated for reducing the error using the inputs information and error values [11].The adaptive filter is able to reduce to noise but could not completely remove the noise from the signal. Increasing the order of filter and selecting new learning factor could improve the noise cancellation performance and signal to noise (SNR) values in practical applications [12].

4. RESULT AND DISSCUTIONS

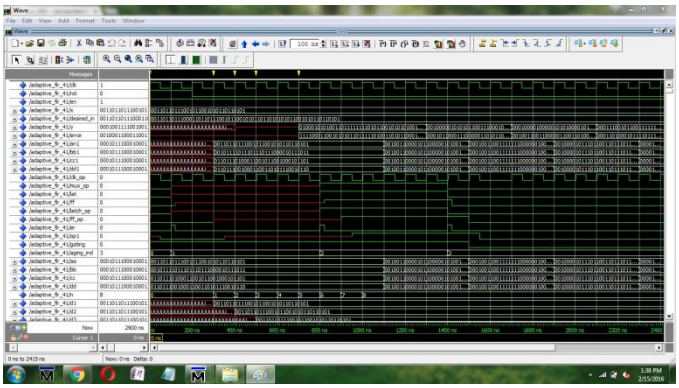

FIG.4.Output diagram
Y[n]

5. CONCLUSION

The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. If a wire becomes narrower, the resistance and delay of the wire will be increased, and in the end, electro migration may lead to open circuits. This issue is also more serious in advanced process technology because metal wires are narrower, and changes in the wire width will cause larger resistance differences. If the aging effects caused by the BTI effect and electro migration are considered together, the delay and performance degradation will be more significant. Fortunately, our proposed variable latency multipliers can be used under the influence of both the BTI effect and electro migration.

In addition, our proposed variable latency multipliers have less performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electro migration and use the worst case delay as the cycle period.In future, the implementation of adaptive digital LMS and DLMS FIR filters on FPGA chips and comparing the behavior of algorithms in terms of chip area utilization and the filter critical path time or filter frequency.

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BIOGRAPHIES

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