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VHDL Synthesis for the Detection of Vitreous Hemorrhages caused by Diabetic Retinopathy

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Abstract - *Diabetic retinopathy is a serious problem occurring to human-beings now-a-days and it is very important to detect it at a very early stage otherwise it may lead to loss of vision. Vitreous hemorrhages is a problem of diabetic retinopathy which occurs in the retina of the eye. Vitreous is a clear gel like structure which fills the retina of the eye and vitreous hemorrhages is disease occurring in the vitreous region of the eye. In this paper sobel edge detector based on VHDL synthesis is proposed. The main aim of this paper is to mainly detect the edges with the help of Xilinx System Generator. The complete design shows the sobel edge detector with the help of Xilinx System Generator, MATLAB and Simulink. The VHDL code is synthesized using Xilinx System Generator. Further the VHDL code is generated using Xilinx ISE design suit 13.*

Key Words: Sobel edge detector, Xilinx System Generator.

1. INTRODUCTION

Diabetic eye disease comprises a group of eye conditions that mark people with diabetics called diabetic retinopathy. Diabetic retinopathy consists of two types they are Non Proliferative Diabetic Retinopathy and Proliferative Diabetic Retinopathy Non-proliferative diabetic retinopathy (NPDR) is the early stage of the Diabetic Retinopathy in which symptoms will be very less or non-existent. In NPDR, the blood vessels in the retina are damaged causing small swells called micro-aneurysms to protrude from their walls. The micro aneurysms may leak liquid into the retina, which may lead to swelling of the macula.
Proliferative diabetic retinopathy (PDR) is the more radical form of the disease. Circulation problems cause the retina to become oxygen rundown. As a result new blood vessels begin to rise in the retina and into the vitreous, the gel-like fluid that fills the back of the eye. The new blood vessel may drip blood into the vitreous, clouding vision. Vitreous hemorrhages implicates changes to retinal blood that cause the retina to bleed or leak the fluid, distorting vision. Therefore it is essential to detect the diabetic retinopathy at an early stage. The proposed method utilizes the sobel edge detector with the help of Xilinx system generator. By the use of edge detection we can obtain some basic information such as location of objects present in the image, their size is calculated, image enhancement and sharpening. The time consumption of this edge detector is less and more accurate results are obtained.
The sobel edge detector is one of the multi-stage algorithm due to its good edge detection capability. The computational time of the sobel edge detection is less as compared to Canny, Prewitt , Roberts and Laplacian. This method is fast multilevel edge detector which utilizes Spartan-3 FPGA. There is an implementation of distributed sobel edge detector on FPGA which uses Xilinx Vertex – 5 FPGA.

2. Proposed Method

Sobel edge detection using Xilinx system generator utilizes various methods .The first method is to load the original image and the second method is to detect the edges are detected and then the VHDL synthesis and VHDL co-simulation is done.

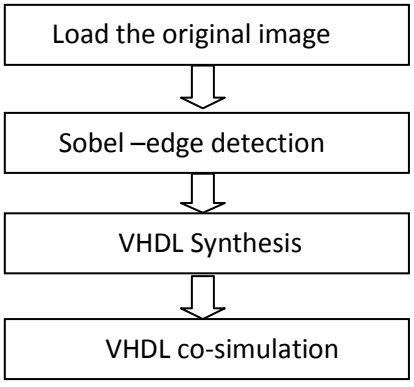

Fig1:- Block diagram of sobel edge detection using VHDL synthesis.

2.1 Sobel –edge detector

The sobel operator performs 2D spatial gradient magnitude on image and so emphasizes regions of high spatial performance that corresponds to edges.

Normally it is used to find the approximate absolute gradient magnitude at every point in a gray scale image.

The sobel operator consists of 3×3 convolution kernels as shown in Figure 2. Each kernels are rotated by 90 degrees.

-1	0	+1
-2	0	+2
-1	0	+1

Gx

+1	+2	+1
0	0	0
-1	-2	-1

Gy

Fig2: convolution of sobel edge detector

These kernels are applied separately to the input image, to create separate measurements of the gradient element in each orientation (call these *Gx* and *Gy*). These kernels are designed to rejoin maximally to edges running vertically and horizontally to each of the pixel grid, one kernel for each of the two perpendicular directions.. The gradient magnitude is given by:

$$|G| = \sqrt{Gx^2 + Gy^2} \quad \text{..... (1)}$$

A predictable magnitude is computed using:

$$|G| = |Gx| + |Gy| \quad \text{..... (2)}$$

which is much faster to compute.

Finally breaking up of the edges is performed with the help of sobel edge detector.

2.2 VHDL Synthesis.

The implemented design is needed to be synthesized in ISE Design Suit 13.1. It creates device deployment summary for hardware implementation.

2.3 Hardware co-simulation

A code generation option that allows to authenticate working hardware and accelerates simulation in Simulink and Matlab. Xilinx System generator supports JTAG communication between a hardware platform and Simulink.

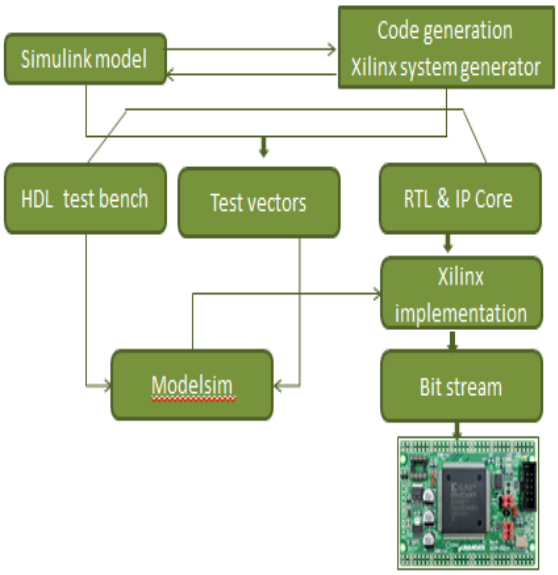

Fig3:-hardware co-simulation using XSG

3. Pre-Processing Steps

This method utilizes the Xilinx System generator which utilizes the Xilinx block-sets for image filtering.
Xilinx system generator is one of the industry important high level tool for manipulating high performance DSP systems using Xilinx. These develop high systems with the industry's most innovative FPGA. It provides system modeling and spontaneous code creation from Simulink and Matlab. It also provides integration with RTL , embedded, Matlab and hardware components of a DSP system. JTAG co-simulation support for virtex -5 family is enhanced to utilize and improve performance.

3.1 Sobel edge detection using XSG

The model base design uses Xilinx block-sets. Sobel edge detector uses 5 line buffer, a sequential stream of pixels to constructs 5 lines of output. Further it uses 5×5 filter. It is executed by using 5n-tap MAC FIR filters. Nine unlike 2-D filters have been on condition that to filter gray-scale images.

The primary advantages of the Sobel operator lie in its easiness. The Sobel method provides an approximation to the gradient magnitude. It can detect edges and their orientations.
The main disadvantage of Canny edge detector is that it is time consuming, due to its difficult computation.

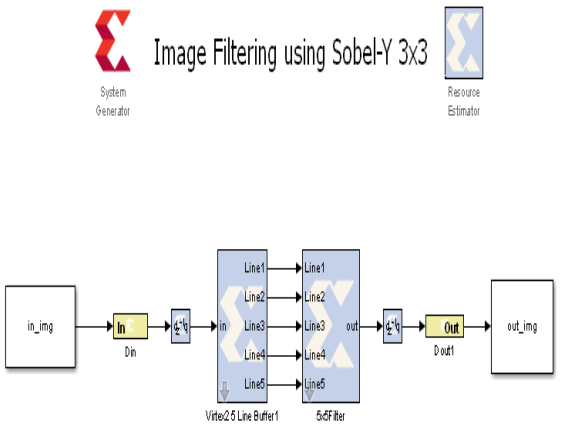

Fig4:- sobel edge detector using XSG

3.2 Setting code generation for XSG

By utilizing HDL coder, multiple XSG subsystems can be designed , but XSG should have same port settings.

HDL coder supports XSG code generation with the following settings

1. Hardware description language should have the same as target language set as in HDL coder.
2. Compilation should be HDL net-list.
3. Create test bench should be unchecked.
4. Synthesis strategy should be XST default.

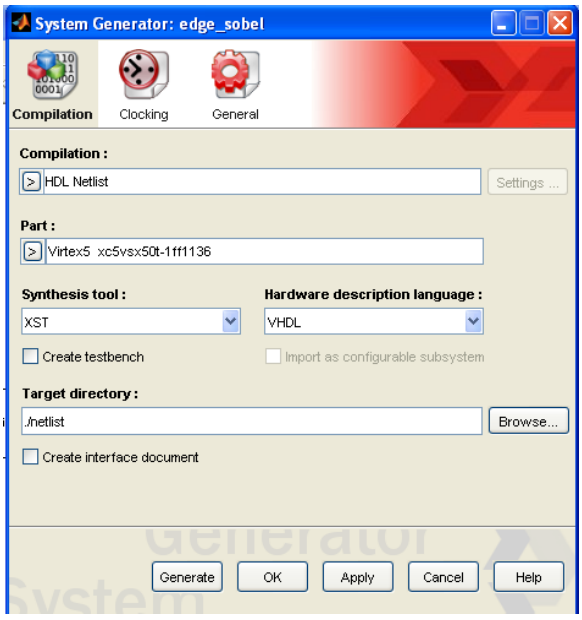

Fig5:-system generator block.

4. Results

The proposed method utilizes Xilinx system generator along with Matlab which also utilizes Xilinx block-sets.

The final results are obtained with the help of Xilinx system generator and sobel edge detector after the VHDL synthesis are shown in figure5. The device utilizes the virtex-5 starter kit.

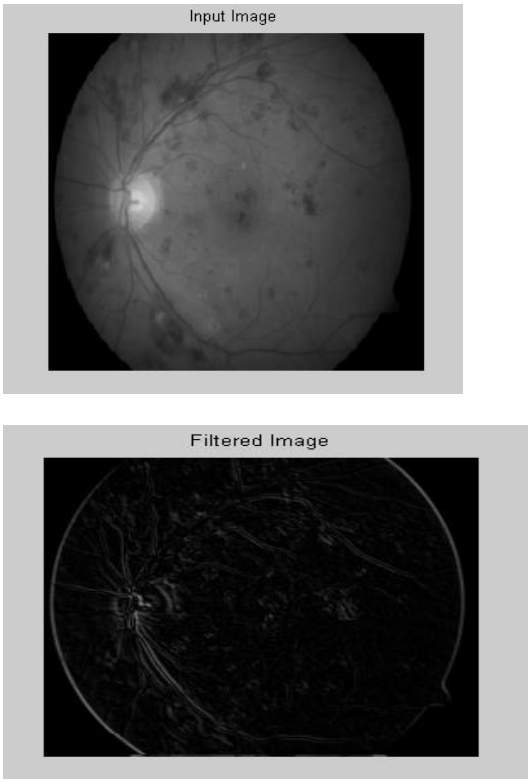

Fig6:-results obtained after VHDL co-simulation.

The proposed method utilizes the lower complexity and it also improves efficiency. It also provides low hardware cost compatibility.

4.1 Hardware Results

The hardware based implementation of detector results is carried out with the help of Xilinx family using Spartan 3 FPGA kit. The software is designed using the Xilinx ISE design suit 13.1. with the support of Xilinx system generator a bit file is generated which is dumped on Spartan 3 FPGA kit in addition to MATLAB. The board used for implementation is shown in figure 6.

Fig7:- Spartan -3E

Table 1:- Device Utilization.

Sr .no	Resource	Referred	utilization
1.	Slice registers	405	1%
2.	LUTs	180	1%
3.	Slice flip-flop	173	1%
4.	Memory	95	1%

5. Conclusion

The proposed work gives better results as compare to canny, Prewitt, Robert and Laplacian because these methods utilizes more computational time . The results obtained with the sobel edge detector are comparatively better. These technique is updated with the help of Xilinx ISE design suit 13.1. The implemented design is targeted on Vertex5 xc5vsx50t-1ff1136 starter kit. This method is very useful in medical images to detect the disease.

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