International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 03 Issue: 04| Apr -2016 www.irjet.net p-ISSN: 2395-0072

A Robust Low Power 512x8 SRAM Based Architecture Using TCAM Functionality

S.Md.Imran Ali[1], Syed Noorullah[2], G.Swetha[3] , D.Venkata Ramana[4]

[1]Assistant Professor, Dept, of ECE, BRINDAVAN Institute Of Technology & Science-KNL, A.P, India
[2] Assistant Professor, Dept, of ECE, SAFA College Of Engineering & Technology-KNL, A.P, India
[3] Student, Dept, of ECE, BRINDAVAN Institute Of Technology & Science-KNL, A.P, India
[4] Student, Dept, of ECE, BRINDAVAN Institute Of Technology & Science-KNL, A.P, India

---

Abstract - *High-speed lookup operations are performed by Ternary Content addressable memories in a deterministic time. TCAMs are limited due to very slow access time, less storage density, low scalability, complex circuitry, and are very expensive in comparison with static random access memories (SRAMs). The benefits of SRAM are available by configuring an additional logic to enable SRAM to behave like a TCAM. T-SRAM is proposed novel memory architecture that emulates the TCAM functionality with SRAM. The Classical TCAM table along columns and rows into hybrid TCAM sub tables are logically partitioned by T-SRAM, which are then processed to map on their corresponding memory blocks. A 512x8 T-SRAM is implemented that consumes 0.024 W of power.*

Key Words: **TCAM, LUT, PE, SRAM**

1.INTRODUCTION

Ternary content addressable memory is an outgrowth of random access memory. TCAM permits its memory to be sought by contents instead of by a location and a memory area among matches is sent to the yield in a steady time. A regular TCAM cell has two static irregular access memory (SRAM) cells and an examination hardware and can store three states – 0, 1, and x where x is a don't care state. The x state is constantly viewed as coordinated regardless of the data bit. The steady time pursuit of TCAM makes it a suitable hopeful in various applications, for example, system switches, information pressure, continuous example coordinating in infection location, and picture handling.

TCAM gives single clock lookup; in any case, it has a few weaknesses contrasted and SRAM. TCAM is not subjected to the serious business rivalry found in the market of the RAM. TCAM is less thick than SRAM. The comparator's hardware in TCAM cell adds multifaceted nature to the TCAM design. The proposed TCAM may be used in network based systems. The access time of TCAM, which is 3.3 times longer than the SRAM access time. Natural design obstructions additionally confine the aggregate chip limit of TCAM. Complex combination of memory and rationale additionally sets aside a few minutes devouring. It has extra logic and capacitive loading due to parallel lengthen of the access time. Further more, the expense of TCAM is around 30 times more for each piece of capacity than SRAM. RAM is accessible in a more extensive assortment of sizes and flavors, is more bland and broadly accessible, and empowers to maintain a strategic distance from the substantial authorizing and eminence costs charged by some CAM sellers. CAM has a very limited pattern capacity.CAM gadgets have exceptionally restricted example limit the CAM innovation does not advance as quick as the RAM innovation.

2. LITERATURE SURVEY

The methods being used hashing to fabricate CAM from RAM however these strategies experience the ill effects of impacts and container flood. In the event that numerous records have been put in a flood range, then a lookup may not complete until numerous basins are sought. In when put away keys contain don't care bits in the bit positions utilized for hashing, then such keys must be copied in various basins, which require expanded limit. Then again, if the inquiry key contains don't care bits, which are taken by the hash, work, various pails must be gotten to that outcomes in execution corruption.

In the execution of the strategy turns out to be effortlessly degradable as the quantity of put away components increments. However, it copies twofold CAM, not TCAM. In this manner, hashing can't give deterministic execution inferable from potential crashes and is wasteful in taking care of trump card.

The strategy proposed RAM and CAM to build up the CAM usefulness. This methodology makes segments of the classical TCAM table utilizing some recognizing bits as a part of CAM passages. However, making parcels of absolutely arbitrary information is an extremely dreary and tedious employment. Since the technique utilizes TCAM as a part of the general design, it brings the characteristic TCAM hindrances in the general engineering. T-SRAM is generic and it has an easy partitioning scheme.RAM-based CAMs showed in have an exponential increment in memory size with the expansion in number of bits in CAM word, in this

way making them restrictive. If a CAM word has 36 bits, its size would be 2^36= 64 GB in . Besides, the technique in just takes a shot at rose information however in run of the mill CAM applications information are absolutely arbitrary. By orchestrating the information in rising request, the first request of passages is irritated. In the event that unique locations are viewed as, the memory and force necessities further increment.

A CAM is an uncommon kind of cache memory TCAMs are one level higher than CAM since they can seek obscure bits additionally i.e. ternary states. The fundamental part of ternary content addressable memory (TCAM) is to hunt information against the pre-stacked information and yield the correlation result which is then used to conjure a related passage from an ordinary memory. A TCAM cell has a cover cell, information cell, and concealing and correlation hardware. Cover and information cells are regularly actualized with SRAM. TCAM is an outgrowth of RAM, which got to be main stream in the writing for its rapid pursuit operation.

The significant utilization of TCAM is in IPv6.Other applications are in system switches, reserve memory, ATM switches, network routers, data compression, real time pattern in virus detection, intrusion detector system, Translation look-a-side Buffers (TLB) in chip.

The bit based TCAM plan comprises of the first information fragment and an additional one-piece section, got from the real information bits. We just get the equality bit, i.e., odd or considerably number of "1"s. The got equality bit is set specifically to the relating word.

3. PROPOSED ARCHITECTURE

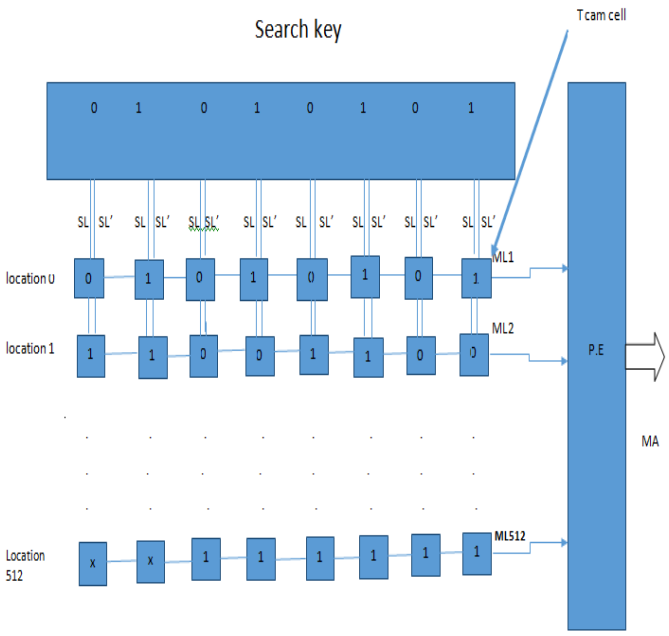

Fig-1: Architecture of T – SRAM

In typical CAM before a search operation is performed, MLs are precharged and SLs are discharged. During a search operation if a comparison circuit and its respective cell does not match the stored bit with the one of its corresponding SLs and the cell ML pull down to low. Even a mismatch in the single bit of mismatch ML. If we apply a search key 1010 to the above figure T-SRAM it find its locations 0 to 3 and the priority encoder select the location 0 as an match address because it has the higher priority. The general design of T-SRAM is portrayed in Fig. 1. where every layer speaks to the engineering appeared in Fig. 2. L layers are present and a encoder (CPE) is needed by CAM). PMA is yielded by every layer. The PMAs are bolstered to CPE, which chooses match address (MA) among PMAs.

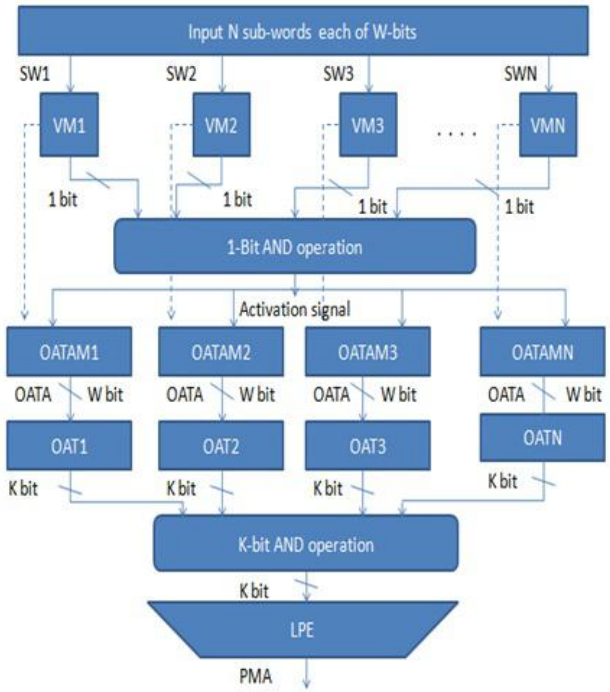

Fig-2: Layered representation of T - SRAM.

N vertical partitions are there in a layer , to accommodate, *N* validation memories and *N* original address tables required to accommodate data in *N* vertical partitions . The layer architecture is equipped with 1-bit AND operation, *K*-bit AND operation, and a layer priority encoder (LPE) to achieve TCAM functionality. Corresponding VM and OAT is present in each hybrid partitioned layer. The VM and OAT constitute a pair. *N* pairs are required for N partitions; each for a hybrid partition in a layer. SRAM units are used along with the additional logic of *K*-bit ANDing, priority encoding and 1-bit ANDing to develop the architecture of T-SRAM. Hence the functionality of 1-bit ANDing, *K*-bit ANDing, and priority encoding constitutes additional logic. Size of each VM is 2^w × 1 bits where w speaks to the quantity of bits in every sub word and 2^wdemonstrates the quantity of columns. A sub expression of w bits suggests that it has all out mixes of 2^w where every blend speaks to a sub word. For instance, if w is of 4 bits, then it implies that there are

aggregate of 2^4 = 16 blends. This clarification is likewise identified with OATAM and OAT. Every sub word goes about as a location to VM. On the off chance that the memory area be conjured by a sub word is high, it implies that the information sub word is available, generally missing. Consequently, VM approves the information sub word, in the event that it is available. In one bit AND operation it ANDs the yield of all VMs. The yield of 1-bit AND operation chooses the continuation of a pursuit operation. On the off chance that the after effect of 1-bit AND operation is high, then it allows the continuation of an inquiry operation, generally confound happens in the relating layer. Each OATAM is of 2^w × w bits where 2^w is the quantity of lines and every column has w bits. In OATAM, a location is put away at the memory area listed by a sub word and that deliver is then used to conjure a line from its relating OAT. In the event that a sub word in VM is mapped, then a comparing location is additionally put away in OATAM at a memory area got to by the sub word. The yield of OATAM is called as OATA. Dimensions of OAT are 2^W× K where w is the quantity of bits in a sub word, 2^w speaks to number of columns, and K is the quantity of bits in every line where every piece speaks to a unique location. Here K is a subset of unique locations from ordinary TCAM table. It is OAT, which considers the capacity of unique locations. K - bit AND Operation It ANDs a little bit by bit the read out K-bit columns from all OATs are read out there corresponding subwords, which are then anded and the result is forwarded to LPE. PMA is present in the result of k bit and operation. Layer Priority Encoder chooses PMA among the yields of K-bit AND operation.

4. SIMULATION RESULTS

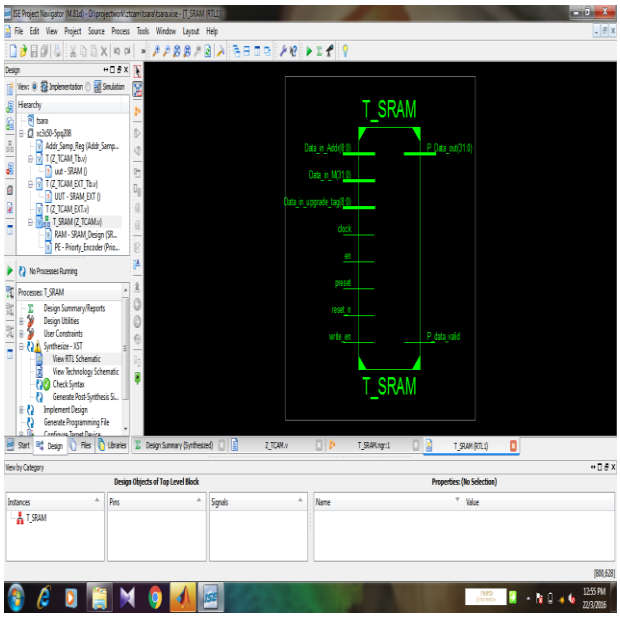

Fig-3: 512X8 T-SRAM Layout

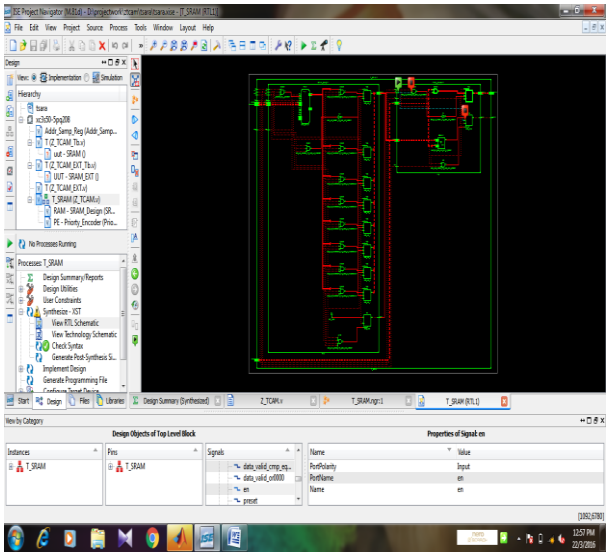

Fig-4:512X8 T-SRAM Detailed layout Layout

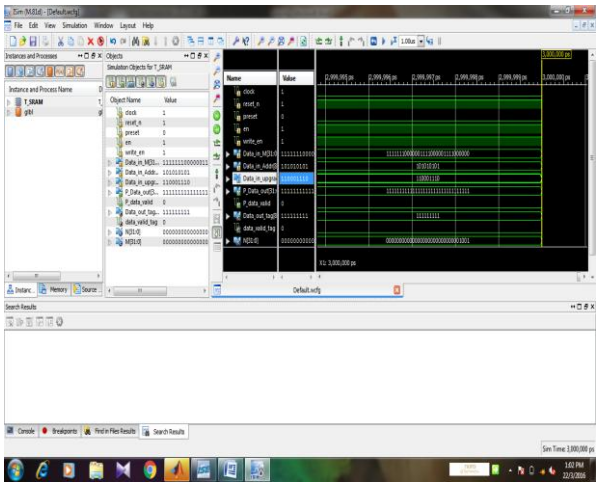

Fig-4: Output of 512X8 T-SRAM For Input 101010101

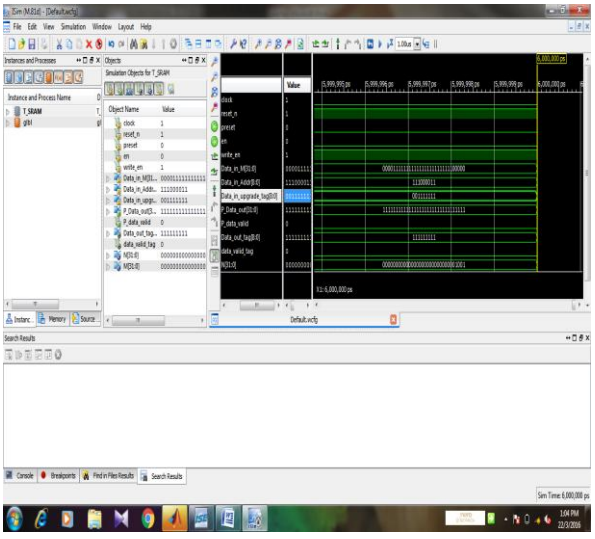

Fig-6: Output of 512X8 T-SRAM For Input 111000011

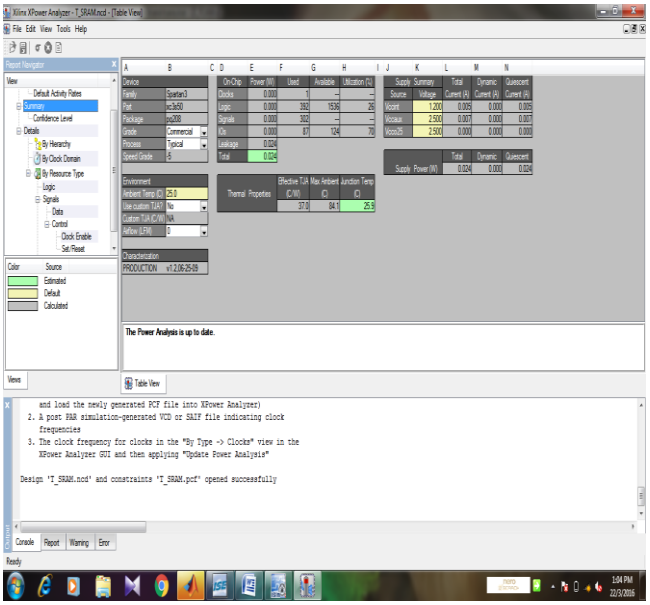

Fig-7: Power Analysis Report

5. CONCLUSION & FUTURE SCOPE

A robust SRAM-based TCAM engineering of T-SRAM is introduced. We have actualized outlines of 512x8 T-SRAM on Xilinx .SRAM-based TCAM is a rich field of exploration and further examination is important to discover more SRAM-based TCAMs. The T-SRAM architecture consumes 0.024w of power to undergo search operations. Our future work intends to examine the field inside and out and accomplish more plans for SRAM-based TCAM which will be helpful in furthur increasing speed of search operations

REFERENCES

[1] N. Mohan, W. Fung, D. Wright, and M. Sachdev, "Design techniques and test methodology for low-power TCAMs," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 14, no. 6, pp. 573–586, Jun. 2006.

[2] P. Mahoney, Y. Savaria, G. Bois, and P. Plante, "Parallel hashing memories: An alternative to content addressable memories," in Proc. 3rd Int. IEEE-NEWCAS Conf., Jun. 2005, pp. 223–226.

[3] S. Dharmapurikar, P. Krishnamurthy, and D. Taylor, "Longest prefix matching using bloom filters," IEEE/ACM Trans. Netw., vol. 14, no. 2, pp. 397–409, Apr. 2006.

[4] D. E. Taylor, "Survey and taxonomy of packet classification techniques," ACM Comput. Surveys, New York, NY, USA: Tech. Rep. WUCSE-2004-24, 2004.

[5] P. Mahoney, Y. Savaria, G. Bois, and P. Plante, "Transactions on highperformance embedded architectures and compilers II," in Performance Characterization for the Implementation of Content Addressable Memories Based on Parallel Hashing Memories, P. Stenström, Ed. Berlin, Germany: Springer-Verlag, 2009, pp. 307–325.

[6] S. V. Kartalopoulos, "RAM-based associative content-addressable memory device, method of operation thereof and ATM communication switching system employing the same," U.S. Patent 6 097 724, Aug. 1, 2000.

[7] W. Jiang and V. Prasanna, "Scalable packet classification on FPGA," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20, no. 9, pp. 1668–1680, Sep. 2012.

Mr.S.MD.Imran Ali has pursued his B.Tech from SAFA College of Engg.& Tech, Kurnool and M.Tech from SKTMCE , Kondair. Presently he is working as Asst.Prof in Dept of ECE of Brindavan Institute of Technology & science, Kurnool.

Mr.Syed Noorullah has pursued his B.Tech from SAFA College of Engg.& Tech, Kurnool and M.Tech from SKTMCE , Kondair. Presently he is working as Asst.Prof in Dept of ECE of Safa College of Engineering , Kurnool.

Mr G.Venkata Ramana is pursuing his B.Tech In ECE Department of BITS-KNL,India

Miss G.Swetha is pursuing her B.Tech In ECE Department of BITS-KNL,India