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IMPLEMENTATION OF SHIFT REGISTER USING DOUBLE EDGE TRIGGERED FLIP-FLOP

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Abstract: *The Shift register can be designed by using double edge triggering method. This double edge triggering method responds at both the edges of the clock applied. So that the shift register can perform faster. In addition clock branch sharing scheme is used with this method. This CBS_ip design has an improvement of up to 20% and 12.4% in view of power consumption and PDP, and also it reduces the number of clocked transistors in the design. It employs conditional discharge and split-path techniques to further reduce switching activity and short-circuit currents, respectively.*

Keywords: Shift Register, Double edge, flip-flop,low power, CBS_ip.

I.INTRODUCTION

A SHIFT register is the basic building block in a VLSI circuit. Shift registers are commonly used in many applications, such as digital filters, communication receivers, and image processing ICs. In image processing as the word length of the shifter register increases, the area and power consumption of the shift register become important design considerations. Shift registers are a type of sequential logic circuit, mainly for storage of digital data. They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop. Most of the registers possess no characteristic internal sequence of states. All flip-flop is driven by a common clock, and all are set or reset simultaneously.

II.TECHNIQUES FOR IMPLEMENTING DOUBLE EDGETRIGGERED FLIP-FLOPS

The art of DEFF and categorize into three groups: conventional DEFF, explicit pulsed DEFF, and implicit pulsed DEFF. For these three categories, the analysing has been going to the clock pulse generating scheme as well as the data latch scheme. The DEFF design will use more clocked transistors than Single edge triggered (SEFF) design generally. However, the DEFF design should not increase the clock load too much. The DEFF Design should aim at saving energy both on the distribution network (by halving the frequency) and flip-flops. It is preferable to reduce circuits 'clock loads by minimizing the number of clocked transistors. Furthermore, circuits with reduced switching activity would be preferable. Low swing capability is very helpful to further reduce the voltage on the clock distribution network for power saving, if applicable. Due to the fact that voltage scaling can reduce power efficiently, the cluster voltage scaling(CVS) systems are widely used.

III. CLOCK BRANCH SHARING IMPLICITPULSED FLIP-FLOP (CBS_IP)

Conventional DEFFs duplicate the area and the load on the inputs. Explicit pulsed DEFFs use external clock pulse generators, which increase the power. In addition, explicit pulsed DEFFscan not work with dynamic logic. SPGFF uses implicit pulsing; however, it has four internal redundant switching nodes. UnlikeSPGFF, DECPFF eliminates the redundant switching activity, however, the number of clocked transistors reaches 21, and the clock branch duplicating structure is complex. To ensure efficient implementation of double-edge clock triggering in an implicit pulsed environment

and to overcome the problem with previous implicit pulsed flip-flops which is the large clock load, a novel clock branch sharing topology is proposed.

The sharing concept is similar to the single transistor clocked FF and another clock branch sharing flip-flop. In this new clock branch sharing scheme, Fig.1CBS_ip, the two groups of clocked branches in the previous clock branch separating scheme (DECPFF) are merged; (N1, N3), (N2, N4) are shared by the first stage and second stage (in the doted circle).Note that a split path (node X does not driven MOS N6 of the second stage, which is in the output discharging path) is used to ensure correct functioning after merging. The advantage of this sharing concept is reflected in reducing the number of transistors required to implement the clocking branch of the double-edge triggered implicit-pulsed flip-flops. Without this sharing, the number of clocked transistors would be much larger than the number of transistors used with the sharing concept. Recall that clocked transistors have a 100% activity factor and consume a large amount of power. Reducing the number of clocked transistorises an efficient way to decrease the power. Using Pseudo nMOS (always on pMOS P1) in CBS_ip takes advantage of the fact that D and Qb have inversed polarity resulting from the conditional discharge technique.

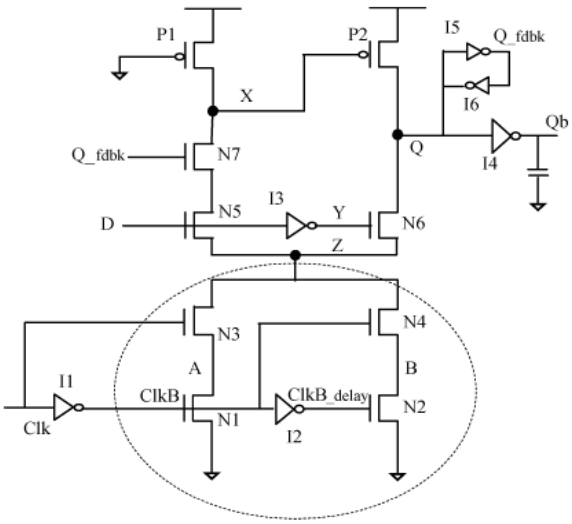


Fig.1 CBS_ip

The discharging path only stays ON for a short while, yielding only a little short circuit current. An inverter is placed after Q, providing protection from direct noise coupling. The double edge triggering operation of the flip-flop, Fig.1CBS_ip, is as follows. Q_fdbk is used to control N7. When CLK rises, CLKB will stay high for a short interval of time equal to one inverter delay. During this period, the clocked branch (N1 andN3) turns on and the flip-flop will be in the evaluation period. Note that the other clocked branch (N2 and N4) is disconnected.

When CLK falls, CLKB will rise, and CLKB_delay will stay HIGH for one inverter delay period during which the transistorsN2 and N4 are both on, and the flip-flop is in the evaluation mode. The first stage in the design is responsible for capturing input transitions of D. The internal node X will discharge causing the outputs Q and Qb to be HIGH and LOW, respectively;N7 turnoff by ; If the input D stays "1,"the first stage is disconnected from ground in the later evaluations preventing node X from experiencing redundant switching activity. The second stage, on the other hand, is responsible for capturing the input transitions. In this case, the falling transition of the input will cause the pull down network of the second stage to be ON and, thus, forcing the output nodes Q andQb to be 0 and 1, respectively. Using a split path in CBS_ip (P2 is driven by X, N2 by Irrespectively), the capacitance on node X is much smaller than that on node Q, which causes a significant difference in propagation delay through the FF. The reason for this is that node Xonly drives one device, P2. To further reduce latency, clocked invertersI1 and I2 are placed to drive bottom clocked transistorsN1 and N2, respectively. Before the clock rising/falling edge, the output of I1/I2 turns on N1, N2, respectively, thus, the internal nodes A and B are discharged to ground before evaluation correspondingly, and this can reduce the discharge time.

Though it has four stacked transistors in the first stage, the above methods (split path, and

moving the early signals near GND)help to reduce the high stack's negative effect on delay.

Using the conditional discharge technique, Q_fdbk turns offN7 in two gate delays, so we need not use a 3-inverter delay in the clock pulse window. The one inverter window width insufficient for node X to discharge to ground. The reasons areas follows. First, node X has a much smaller capacitive load than that at Q. Further, we can adjust the one-inverter-delay by weakening the nMOS in I1 and I2. Note that the nMOS in I2and I1 control the gate of N1 and N2. Weakening of the nMOScan be achieved by using the width , and increasing the length (L) of the nMOS (since the resistance is proportional to L/W). So, when L increases, the resistance increases. This allows N1 and N2 to stayONlonger after the clock rising/falling edge, respectively, before being turned off by the nMOS in I1and I2, thus, enlarging the pulsewidth.For the four stacked transistors, N5, N1, N3, and N7, charge sharing may occur when three of them become ON at the sometime. A properly sized always-ON pMOS P1 enables a constant charging path, which reduces the effect of charge sharing. P1,N1, N2, and N3 should be properly sized to ensure a correct noise margin; the value of VOL should be small.

In summary, the clock-sharing scheme reduces the number of clocked transistors. The reduction of the number of clocked transistors reduces the switching activity, decreasing the power usage. Also, the pseudo-nMOS replaces the pMOS clocking scheme. In addition, the conditional discharge technique and split path technique are used to reduce redundant switching activity at node X and reduce the short circuit power consumption, respectively.

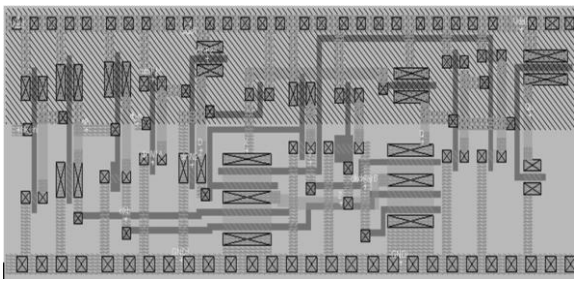


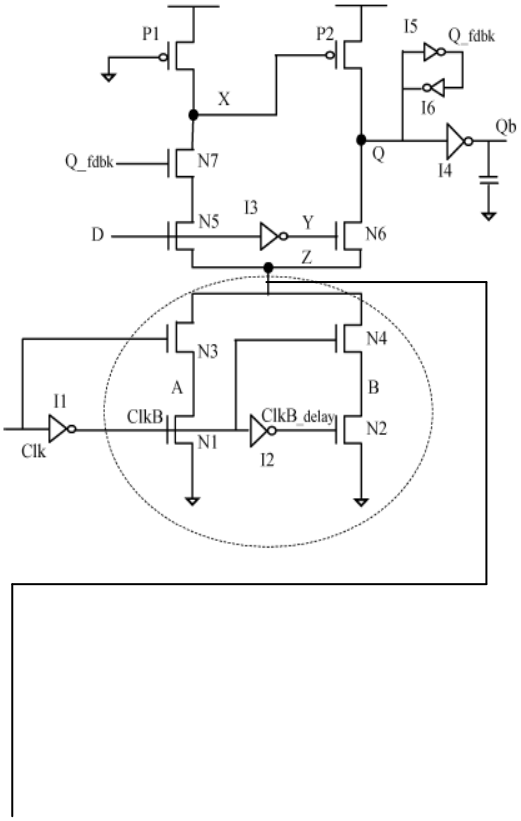
Fig.2 Layout of CBS_ip

IV.ARCHITECTURE OF SHIFT REGISTER WITH PROPOSED METHOD

The architecture of the shift register is designed with flip-flops(master- slave) with DEFF CBS_ip is shown in the Fig.3.

The operation of CBS_ip was given above. With that it combines with DEFF and gives the DEFF CBS_IP total performance. Then the Shift register is combined here for evaluating the performance with the proposed.

The output of the DEFF CBS_ip has been given to the shift register where it starts to operate its shifting operation. And the total operation performance simulation results are shown below. While evaluating it shows better performance with the improvement of up to 20% and 12.4% in view of power consumption and PDP.



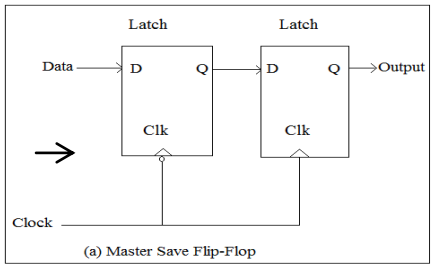


Fig.3 Shift register with DEFF CBS_ip

V.SIMULATION RESULTS

Simulated Waveforms of the Proposed Shift Register

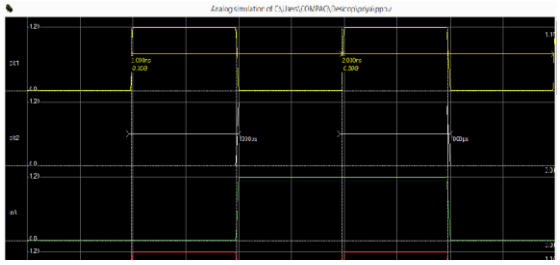


Fig.4

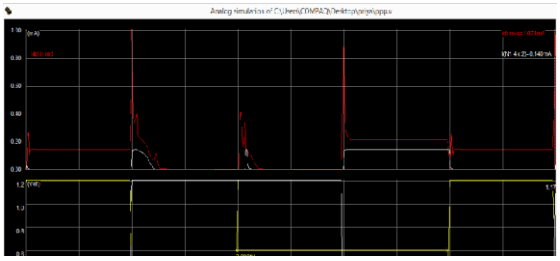


Fig.5

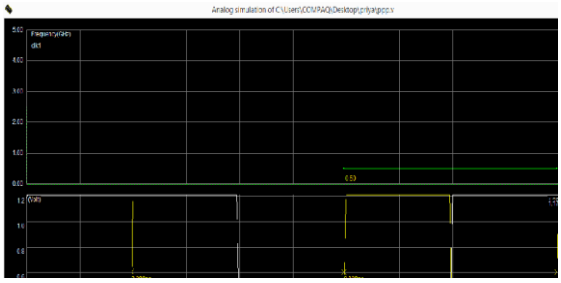


Fig.6

VI.CONCLUSION

The proposed CBS_ip uses a clock branch sharing scheme to sample the clock transitions, which efficiently reduces the number of clocked transistors and results in lower power while maintaining a competitive speed. It employs the conditional discharge technique and the split path technique to reduce the redundant switching activity and short circuit current, respectively. The CBS_ip flip flop has the least number of clocked transistors and lowest power; hence, it is suitable for use in high-performance and low-power environments. It combines with double edge triggered flip-flop where the DETFF responds at both the positive and negative edges, so that the operation speed increases with reduced power consumption. This design has an improvement of up to 20% and 12.4% in view of power consumption and PDP.

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