International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 03 Issue: 04 | Apr-2016 www.irjet.net p-ISSN: 2395-0072

CLOCKED LOW POWER HIGH SPEED REGENERATIVE DOUBLE TAIL COMPARATOR

SASIKALA.P[1] ,SARAVANAKUMAR.A[2]

[1]*PG Scholar, M.E (VLSI Design), Dept.of ECE, Gnanamani College of Technology, Namakkal, Tamil Nadu.*

[2]*Assistant Professor, Dept. of ECE, Gnanamani College of Technology, Namakkal, Tamil Nadu.*

Abstract- *Comparator is an important part of Analog to Digital Converter (ADC), used to find out whether input signal is high or low at each clock signal. The need for ultra low-power, area efficient, and high speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. A conventional comparator consisting of two cross-coupled inverters is modified for fast operation and low power by adding few transistors with multi threshold voltage technology. Analysis of power and delay of dynamic comparator are presented. The advantage of this comparator is rail to rail output swing, no static power consumption and robustness against influence of mismatch. Simulation result in 0.18µm confirms reduction in power in proposed double tail comparator.*

Key Words - Double tail comparator, Analog to digital converter, Low power Design, Dynamic clocked comparator.

I. INTRODUCTION

Circuit design in ultra deep sub-micrometer (UDSM) CMOS technology affected from low supply voltages especially

in comparison with threshold voltage of devices and leakage current of circuit. Hence design of high speed comparator is quite difficult for smaller supply voltage, to compensate this larger transistors are needed in given technology. Common mode input range is important for high speed comparator which is also affected by smaller supply voltage because it limits common mode input range. There are so many techniques for low voltage design such as supply boosting methods, body-driven transistors current mode design and techniques using dual-oxide processes.

To eradicate input-range and switching problems there are two methods namely boosting and bootstrapping based on augmenting the supply, reference or clock voltage. Body- driven technique in which body driven MOSFET operates as depletion type device but body driven transistor affected by smaller trans-conductance in comparison with gate driven fabrication technology. New circuit structure helps to eradicate stacking of lots of transistors without increasing complexity, between both rails namely supply rail and ground rail for low supply voltage operation. But there is need of additional circuit for to increase comparator speed for low voltage operation technique. Double tail structure based on separate cross coupled stage and input stage and these separations of cross coupled stage and input stage results in fast operation over supply voltage range and common mode range.

In this paper, analysis made about conventional comparator and proposed double tail comparator. Whereas double tail comparator does not require supply voltage boosted technique or stacking of too many transistors. Latch delay time reduced by adding few transistors to the conventional double tail comparator. Now this reduced delay time also results in power saving.

II.CONVENTIONAL DYNAMIC COMPARATOR

Clocked regenerative comparator provides fast decision by means of using strong positive feedback in latch therefore it is most widely used in high speed ADC. The performance of comparator compared on the basis of parameters such as noise, kick back noise, random decision errors and offset, Schematic diagram shown in fig. 1 is of conventional comparator and its operation consisting of two parts namely reset phase and comparison phase. Reset phase defined as start condition in this condition if CLK = 0 then Mtail is OFF and M7, M8 pulls both output nodes outp and outn to VDD. Whereas in comparison phase if CLK = VDD then both transistors M7 and M8 are OFF and Mtail ON.

During comparison phase both output nodes outp and outn which pre-charge to VDD, start to discharge at different discharging rate depending on level of both input voltage(TNP and INN).

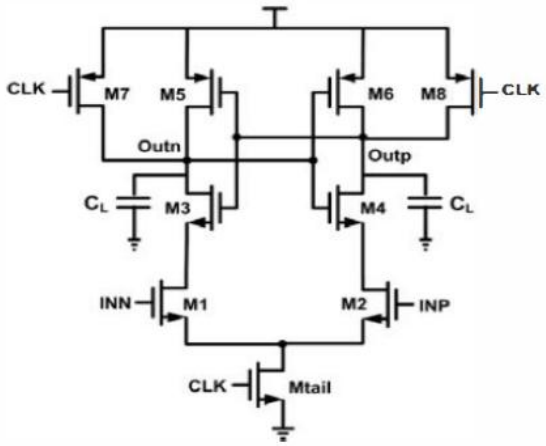

Fig. 1. Schematic of Conventional Dynamic Comparator

Consider, if voltage at INP greater than voltage at INN then firstly M4 ON and hence outp discharge faster than outn. It will initialize latch regeneration which caused by back to back inverter formed with transistors M3-M5 and M4-M6. For voltage at INN greater than INP the circuit works so on.

The delay of conventional comparator consisting of two time delay, first one is delay due to capacitive discharging of load capacitance and second one is due to regeneration of latch. Discharge delay of load capacitance mainly depends on Vth and load capacitance. Whereas regeneration delay of comparator depends on VDD and load capacitance.

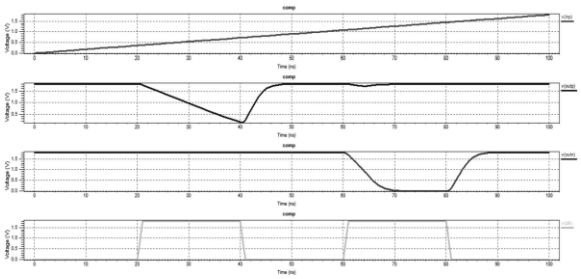

Fig. 2. Simulation of Conventional Dynamic Comparator

The advantage of this structure is rail to rail output swing, no static power consumption, high input impedance and less affected by noise. Whereas disadvantage are several stacked of transistors and high supply voltage that needed to overcome proper delay time. Another most important drawback of this conventional comparator is there is that onlyone current path that defines current for both the cross coupled latch and differential amplifier which is via Mtaill. Mtaill operates mostly in triode region depend on common mode voltage which is not favorable for regeneration.

III. CONVENTIONAL DOUBLE TAIL COMPARATOR

The schematic diagram of the conventional double tail comparator is as shown in fig. 3. It can operate in low voltage applications compared to the conventional dynamic comparator.

.

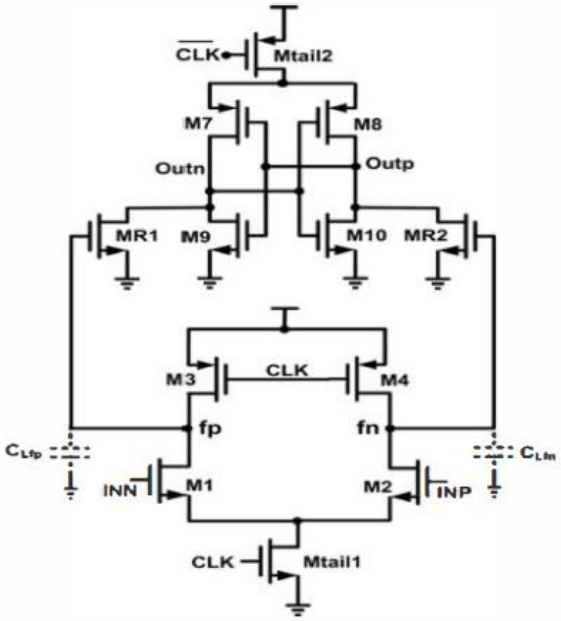

Fig. 3. Schematic of Conventional Double tail comparator

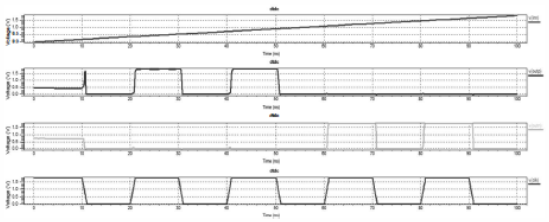

Fig. 4. Simulation of Conventional Double tail comparator

The operation of the conventional double tail comparator is During reset phase that means if CLK =0 then Mtaill and Mtail2 are OFF and M3, M4 pulls fp and fu nodes to VDD resulting both control transistor MCI and MC2 are ON and hence both transistor MRI and MR2, reset both output nodes outp and outn to ground

While in decision phase if CLK = VDD, Mtaill and Mtail2 are ON then M3 and M4 turns off and the both voltage nodes that is fp and fu start to drop at the different drop rate, where drop rate of both nodes depends on drain current of transistor Mtaill. Both intermediate transistors namely MRI and MR2 provides shielding between output and input which also results in reduction of kickback noise. Both intermediate transistors are leads to more power consumption therefore to reduce power consumption of comparator there is need to control both intermediate transistors which are MR1 and MR2 based on input at both input INN and INP. These drawbacks of double tail comparator improved in proposed comparator.

IV. DOUBLE TAIL COMPARATOR FOR HIGH SPEED

Double tail comparator, where its design based on conventional comparator, but this comparator is useful to increase voltage difference between both voltage nodes fn and fp based on respective input at INN and TNP. As shown is schematic diagram both transistors namely MCI and MC2 connected in cross coupled manner are used to increase voltage difference between fu and fP nodes results in increased latch regeneration speed.

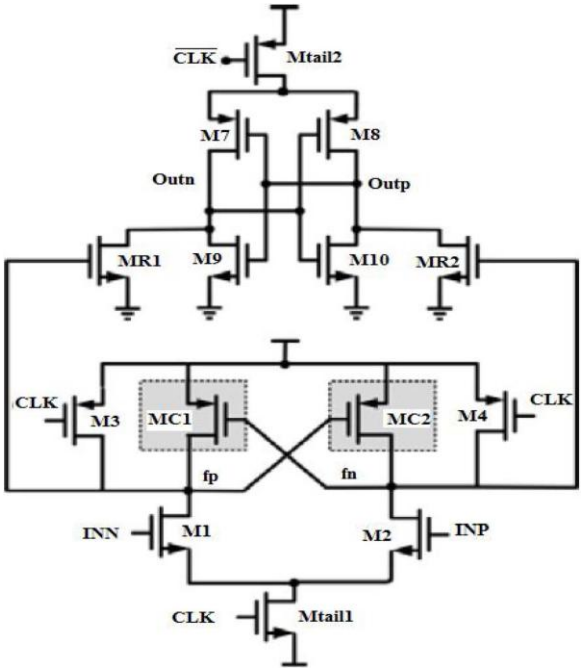

Fig. 5. Schematic diagram of Double tail Comparator for high speed

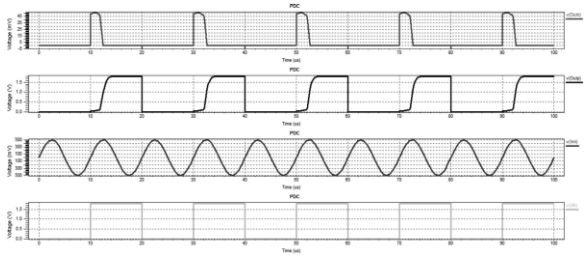

Fig. 6. Simulation of double tail comparator for high speed

The operation of this comparator as, during reset phase that means if CLK =0 then Mtaill and Mtail2 are OFF and M3, M4 pulls tp and fn nodes to VDD resulting both control transistor MC1 and Mc2 are OFF and hence both transistor MR1 and MR2, reset both output nodes outp and outn to ground. While in decision phase if CLK = VDD, Mtaill and Mtail2 are ON. At beginning control transistor are OFF hence tp and fn start to drop at different drop rates depending on voltage at corresponding input INP and INN. If voltage at INP greater than voltage at INN then fu drops faster than fP. Here control transistor used to increase voltage difference by detecting corresponding discharge at node fu or fP. If fu discharge firstly then MCI detects change in input at gate and fP node pre-charge to VDD. For this condition we get high output at node outp and vice versa for voltage at INN greater than voltage at INP. But if any of the control transistor is ON then it gives path to flow of current from VDD to ground this fact resulting static power consumption. This static power consumption is the main drawback of this comparator. Now by adding single transistor below Mtaill then by adjusting threshold of that transistor we can improve power consumption of comparator.

V. PROPOSED DOUBLE TAIL COMPARATOR FOR LOW POWER

Proposed double tail comparator. It gives better performance for low voltage applications, and its design based on the double tail structure. In this circuit two transistors added which results in increasing regeneration speed. These transistors termed as control transistors namely MCI and MC2 which are connected in cross coupled manner.

The operation of the proposed comparator is as shown in figure. During reset phase that means if CLK =0 then Mtaill and Mtail2 are OFF and M3, M4 tp and fn nodes to VDD resulting both control transistor MC1 and Mc2 are OFF and hence both transistor MR1 and MR2, reset both output nodes outp and outn to ground. While in decision phase if CLK = VDD, Mtaill and Mtail2 are ON. At beginning control transistor are OFF hence fp and fn start to drop at different drop rates depending on voltage at corresponding input INP and INN. If voltage at INP greater than voltage at INN then fu drops faster than fp. Here control transistor used to increase voltage difference by detecting corresponding discharge at node fu or fp. If fu discharge firstly then MC1 detects change in input at gate and fp node pre-charge to VDD. For this condition we get high output at node outp and vice versa for voltage at INN greater than voltage at INP.

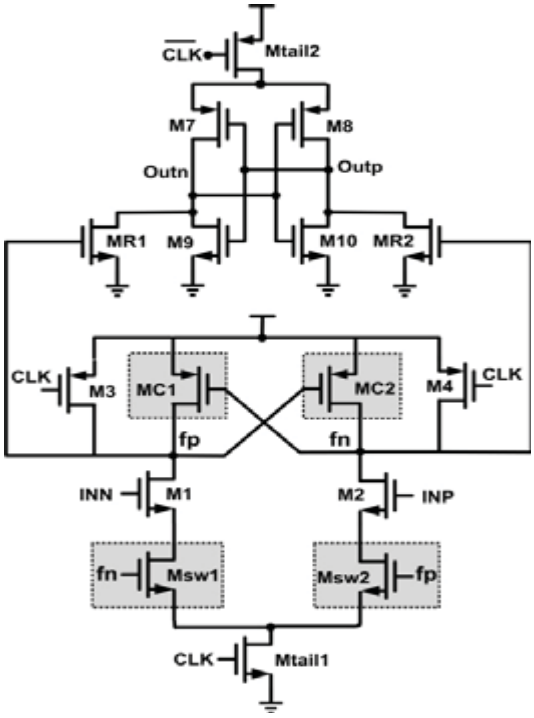

Fig. 7. Schematic diagram of proposed comparator for Low power

To overcome static power consumption due to any of the control transistor two transistors are added namely Msw1 and Msw2, as shown in schematic of this comparator. These two switching transistors are used in comparator to avoid flow of current from VDD to ground due to fact that if any control transistor are ON to avoid static power consumption of the comparator. Now by adding single transistor below Mtaill then by adjusting threshold of that transistor we can improve power consumption of proposed comparator.

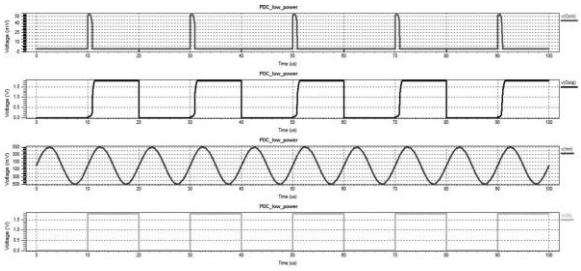

Fig. 8. Simulation of proposed comparator for low power

VI. SIMULATION RESULT

To compare proposed comparator with conventional comparator all circuits are simulated in 0.181l m CMOS technology at VDD = 1.8 V. With this we get average power consumption for conventional comparator is 68.58x10^(-6) Whereas for conventional double tail comparator it is about 1.021x10^(-9) but for proposed comparator the average power is about 0.92xl0^(-9). In this way average power reduced in proposed double tail comparator. Without complicating the circuit just by adding single transistor near ground line by adjusting its threshold voltage power consumption can be improved.

CONCLUSION

Analysis of comparator is presented in which dynamic comparator proposed with high speed in order to improve the performance of the dynamic comparator in terms of power. In this paper the common structure of conventional and double tail comparator are explained and compared the delay and power of those comparators. Pre layout simulation results in 0.181lm CMOS technology confirmed that the average power of modified comparator is reduced.

REFERENCES

[1] Samaneh Babayan-Mashhadi, Reza Lotfi" Analysis And Design Of A Low Voltage Low Power Double-Tail Comparator", IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 22, No. 2, February 2014.

[2] Mesgarani, S. U. Ay"A 1.2-V 100KS/s energy efficient supply boosted SAR ADC", 2013 IEEE.

[3] B . .I. Blalock," Body-Driving As A Low-Voltage Analog Design Technique For CMOS Technology," In Proc. IEEE Southwest Symp. Mixed-Signal Design, Feb. 2000, Pp. 113-118.

[4] M. Maymandi-Nejad And M. Sachdev, "I-Bit Quantiser With Rail To Rail Input Range For Sub-IV Modulators," IEEE Electron. Lett., Vol. 39, No. 12, Pp. 894-895, .Ian. 2003.

[5] Bernhard Goll, Horst Zimmermann "A Comparator With Reduced Delay Time In 65-Nm CMOS For Supply Voltages Down To 0. 65 V", IEEE Transactions On Circuits And Systems-Ii: Express Briefs, Vol. 56, No. II, November 2009.

[6] Samaneh Babayan-Mashhadi, Reza Lotfi "Analysis Of Power In Dynamic Comparators", 2013 IEEE.

[7] Iaeha Kim, Brian S. Leibowitz, .Iihong Ren, Chris.l. Madden" Simulation And Analysis Of Random Decision Errors In Clocked Comparators" IEEE

Transactions On Circuits And Systems-I: Regular Papers, Vol. 56, No. 8, August 2009.

[8] B. Shiva Kumar, Fazal Noorbasha, K. Vinay Kumar, N. V. Siva Rama Krishna. T "Analysis Of New Dynamic Comparator For ADC Circuit", Journal Of Engineering Research And Applications ISSN : 2248-9622, Vol. 4, Issue 5(Version 4), May 2014, Pp. 85-90.

[9] Umamaheswari. V.S, Rajaramya. V. G "Low Power High Performance Double Tail Comparator", 647 International Journal Of Scientific Engineering And Technology (lSSN : 2277-1581) Volume NO. 3 Issue No.5, Pp : 647-650.

[10] Monica Rose .loy, Thangamani M. "Design And Analysis Of Low Power Comparator Using Switching Trans-Istors", IOSR Journal Of VLSI And Signal Processing (lOSR-.IVSP) Volume 4, Issue 2, Ver. 111 (Mar-Apr. 2014), PP 25-30 E-ISSN 2319 - 4200, P-ISSN No. : 2319 – 4197.

[11] S. sivasathya, T.Manikandan" Design Of Double Tail Comparator For High Speed ADC", International Journal Of Innovative Research In Computer And Communication Engineering Vo1.2, Special Issue I, March 2014.

[12] M.Dinesh Kumar, S.lndira "Design Of Double Tail Dyn-Amic Comparator Through Analysis Of Low Power Con-Sumption Of Conventional Dynamic Comparator", 2 International Journal Of Inventions In Computer Science And Engineering ISSN (Online): 2348 - 3539, ISSN (Print): 2348 -3431.