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"Designing of Double Tail Comparator for High Speed Application: A Review"

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Abstract: *Nowadays the comparator becomes of great importance due to its use in analog–to-digital converters. The increasing demand of high speed comparators increases the efficient operations of ADC's. This paper presents the use of the double tail comparator for the faster operation of ADC's. The design of double tail comparator has preamplisfier stage and latching stage. The circuit design of a conventional comparator is modified with a double tail dynamic comparator to reduce the power and voltage by increasing the speed. The technology scaling of CMOS transistors enables low power and low voltage operation which decreases the offset voltage and delay of the comparator. The design is simulated in 0.18um CMOS technology using tanner EDA tools. The major objective of this paper is to reduce the delay of double tail comparator for small supply voltage.*

Key Words: Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs), tanner EDA.

1 INTRODUCTION

Today the need for ultra low-power, area efficient and the high speed analog-to-digital converters is responsible for the use of dynamic regenerative comparators. Analog-to-digital converters (ADC's) translates analogue quantity into digital signals, computing, data transmission and control systems. In today's world the digitized signals are used in almost all fields. For the digitized signal the ADC's plays very important role as ADC's converts the analog signal into digital signal. For this the basic comparator operation is used. The performance of high speed analog to digital converters (ADCs) basically depends on the comparator. The conversion from analog to digital form mostly involves comparator action where the value of analog voltage at some point in time is compared with some standard value. The input to the ADC is a voltage. In ADC the input signal is converted into the digital signal in the form of binary.

1.1 Comparator

Comparator compares two currents or voltages and based on the comparison produces the digital output. The basic function of a CMOS comparator compares a input signal with the reference signal and generates the output accordingly. A comparator consists of a high gain differential amplifier. Comparator is one of the building blocks in most of the analog-to-digital converters without which the process of data conversion cannot take place. In general comparators are very fast. Many high speed ADCs, such as flash ADCs, require high-speed, low-power comparator.

The circuit of comparator is not immune to speed power trade off. A flash ADC's is a high speed device uses transistors with large aspect ratios and hence it consume high power. So depending on the particular application a comparator should be selected. In ultra deep submicrometer CMOS technologies, Hence, this is most challenging to design high-speed comparators when the supply voltage is smaller. Clocked regenerative comparators are fast decision making due to the use of strong positive feedback in the regenerative latch. The designing structure and working of both the comparators (conventional and double-tail comparator) are analysed and presented in this paper.

1.2 Single tail comparator

Clocked regenerative comparators have found wide applications in many high-speed ADCs due to their fast decisions making. The single tail comparator is also known as conventional comparator.

The schematic diagram of the conventional dynamic comparator which is used in analog to digital converters, with high input impedance, static power consumption is not shown in Fig.1. Comparator has two operation modes, first one is the reset phase and second is the comparison or evaluation phase. The modes of operation depend on the clock input given to node. For Clock = 0 known as reset phase and clock = Vdd known as evaluation phase. When clock = 0, nMOS transistor is in off and pMOS transistor is in on. When clock = Vdd, nMOS is in on and pMOS transistor is in off.

a) Reset phase : When clock = 0, the circuit is in reset phase, while Mtail is off. The reset transistors M7 and M8 turns on. The output nodes Outn and Outp are at Vdd due to the reset transistors.

b) Comparison phase: When clock = vdd, the reset transistors M7 and M8 became turn off and Mtail is on. Now Outn and Outp, which had been pre-charged to Vdd, start to discharge. The Discharging rates are different depending on the corresponding input voltage applied at

the nodes INN and INP. Outp discharges rapidly than Outn, hence Output voltages, which had been pre-charged to VDD, it starts to discharge with different discharging rates; depending on the corresponding voltages at INN and INP. Assuming the case where VINP > VINN, Outp discharges more rapidly than Outn, hence when Outp (is discharged by the transistor M2 drain current), falls down to Vdd–|Vthp| before Outn (which is discharged by transistor M1 drain current), the corresponding pMOS transistor will become turn on initiating the latch regeneration. Thus, at Outn gets Vdd and Outp discharges to ground. If VINP < VINN, Outn discharges very fast than Outp and operations performed vice versa.

The delay of this comparator is consists of two time delays, t0 and latch. The delay t0 represents the capacitive discharge of the load capacitance. In case, the voltage at node INP is higher than INN (i.e., VINP > VINN), Outp node gets discharge more rapidly as compared to Outn node because of the drain current of transistor M2**,** which is driven by M1 with smaller current.

High input impedance is the main advantage of Single tail structure, no static power consumption, rail to rail output swing and good robustness against noise and mismatch. Due to the fact that parasitic capacitances of the input transistors do not directly affect the switching speed of the output nodes, it is possible to design large input transistors to minimize the offset. The disadvantage, on the other hand, is that due to several stacked transistors, the delay time of the latch consumes very high supply voltage. Beside this another disadvantage of this structure is that there is only one path for current through tail transistor Mtail, which defines the current for both the latch (the cross-coupled inverters) and the differential amplifier. Due to this there is some delay in the passage current from one node to ground or from one latch to another latch.

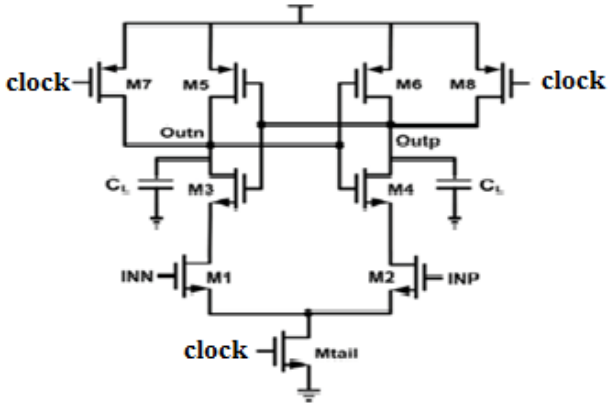

Fig-1: Schematic of conventional dynamic comparator

The design of conventional comparator is simulated on tanner tool with 0.18 um CMOS technology results in less power and less delay of 940 ps with supply of 0.8v.

1.3 Double tail comparator

Double tail comparator is clocked regenerative comparators. Clocked regenerative comparators have found many applications in many high-speed ADCs since they can make fast operations because of its strong positive feedback in the regenerative latch. For its best performance in low voltage application the various comparators are designed based on the double-tail structure.

The designing of double tail comparator has dual input, dual output inverter stage that is suitable for high speed analog-to-digital converters. The double tail comparator also has low voltage and low power. In this technique, the voltage difference between the output nodes is increased for increasing the latch regeneration speed. For maintaining the high speed of proposed comparator, the main idea is to increase ΔVfn/fp.

Fig.2 demonstrates the schematic of the double tail comparator. The Double tail architecture has two tail transistors hence the name is double tail comparator. Double tail comparator is used for low power applications. In this technique, the voltage difference between the output nodes is increased in order to increase the latch regeneration speed. For this, two control transistors are added to the first stage in parallel to M3 and M4 transistors but in a cross-coupled manner. The two modes of operation of double tail comparator are the reset phase and the decision making phase. Depending upon the clock input, the modes of operation is decided. Clock = 0 known as reset phase and clock = Vdd known as evaluation phase. When clock = 0, nMOS transistor is in off state and pMOS transistor is in on state. When clock = Vdd, nMOS is in on and pMOS transistor is in off state.

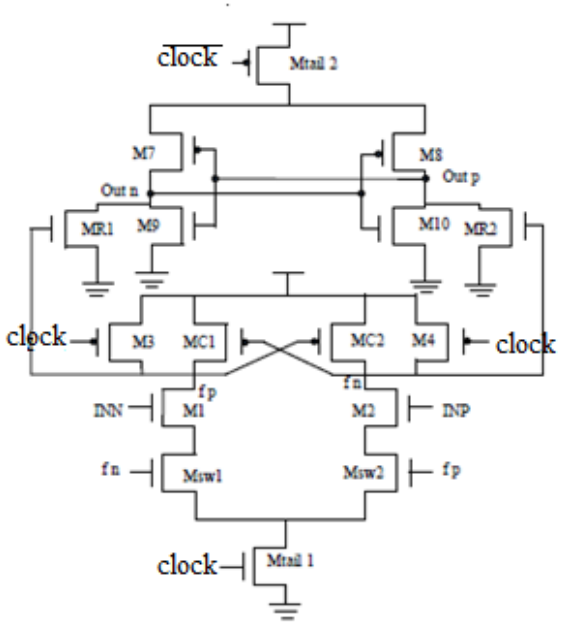

Fig-2: Schematic of double tail comparator

The operation of the proposed comparator is given below. When clock = 0, the reset phase, both the tail transistors Mtail1 and Mtail2 are in off to avoid static power. Transistor M3 and M4 are turns on. M3 and M4 pulls both fn and fp nodes to Vdd, hence both the transistor MC1 and MC2 are cut off. In the circuit MR1 and MR2 are used which are the two intermediate stage transistors. These transistors are used to reset both latch outputs to ground. During decision-making phase, clock = Vdd, both the tail transistors are turns on, M3 and M4 transistors are switched off. During the beginning of this phase, the control transistors MC1 and MC2 are still in off state (since fn and fp are about Vdd). Thus, fn and fp start to drop with different rates depending on corresponding input voltages. Suppose VINP > VINN, so fn Discharge rapidly, (since M1 provides less current than M2). As long as fn continues falling, the corresponding pMOS control transistor (MC1 in this case) becomes turn on, pulling fp node back to the Vdd, thus another control transistor remains turn off, so that fn discharges completely.

As one of the control transistors turns on, a current from Vdd is drawn to the ground through input and tail transistor (i.e., MC1, M1, and Mtail1) that result in static power consumption. To overcome this disadvantage, two nMOS switches are used below the input transistors such as Msw1 and Msw2. At the initial condition of decision making phase, due to the fact that both fn and fp nodes have been pre-charged to Vdd (while the reset phase), both switches are off and fn and fp start to drop with different discharging rates depending on inputs. As soon as the comparator finds that one of the fn or fp nodes is discharging faster, control transistors will act in such a way to increase their voltage difference. Assume that fp is charged up to the Vdd and fn is discharged completely, hence the switch is opened for charging of fp, the complete discharge of fn node is due to the other switch which is connected to fn is closed. In other words, the complete operation of the latch is due to the operation of the control transistors with the switches. The design is simulated using 0.18 um CMOS technology that results in the reduced delay of 294 ps with the supply of 0.8 v.

2 LITERATURE REVIEW

Samaneh Babayan-Mashhadi[1] proposed the delay analysis and its analytical expressions for clocked dynamic comparators. The designing styles of the conventional dynamic comparator and double-tail dynamic comparators are presented. In this paper based on the theoretical results, a new design of dynamic comparator with low-power, low-voltage capability is presented which is used to improve the performance of the comparator. The design of this proposed comparator is simulated using 0.18um CMOS technology and results in reduced delay and energy per conversion to a great extent as compared with the conventional dynamic comparator and double tail comparator.

S.Sivasathya, T.Manikandan[2], the designing of SAR using double tail comparator is presented in the paper and the delay, speed and yield range of the analog to digital converter is analysed. This circuit can be used for all types of ADC's for high speed applications. The layout simulation is done in microwind software 3.1 that confirms the results of analysis of double tail comparator.

N.Bhuvaneswari, V.Gowrishankar, Dr. K. Venkatachalam[3] Proposes the comparison of existing clocked dynamic comparators in different scaling technologies is carried out. As high speed and minimum energy dissipation are the main criteria in day to day portable applications, this paper presents an extensie delay analysis of the comparators which has the significant reduction in delay. Experimental evaluation of the proposed comparator designs shows that the HSDC design show better delay reduction compared to conventional dynamic comparator design.

Monica Rose Joy[4] presented the schematic for the conventional comparator and dynamic double tail comparator. By studying both the circuit analysis ,the proposed comparator is designed .In this papaer the dynamic double tail comparator design is modified by adding few numbers of transistors so that the positive feedback strengthen and it results in reduced delay and power at very small supply voltage.

MadhumathiS, Ramesh Kumar[5] In this paper various circuit of the comparator are presented. The comparator reduces offset voltage, delay, power and provides high speed. A double tail comparator with cascade and parallel connection is proposed. By replacing some transistors in parallel, the offset voltage is reduced. Delay is reduced in parallel connection significantly as

compare with cascade connection. Hence the proposed comparator can be used for high speed ADCs. The CMOS 0.25µm technology used which gives the analysis result, the frequency is 41MHz and given supply voltage is 0.8v

3 PROPOSED WORK

The analysis of delay and power is studied from the papers presented by Samaneh Babayan-Mashhadi, B. Goll and H. Zimmermann as mentioned above. Based on that results we will design the double tail comparator in CMOS technology. The Proposed comparator circuit will have low voltage, low power and delay will be reduced significantly. By adding few numbers of control transistors, the regeneration speed of the latch will be increased which gives the reduced delay. As the delay reduces, power will also be reduced for very small supply voltage. The small supply voltage will be of 0.8v. The proposed comparator will be used in high speed applications where there is need of fast decision making devices. The design layout of the simulation will be carried on the tanner tools 0.18um CMOS technology results in the analysis of parameters of comparator.
The main idea of this proposed comparator is to reduce the delay for its use in ADC's.

4 EXPECTED OUTPUT

By comparing the conventional comparator and dynamic double tail comparator in the literature review it is found that shorter the propogation delay, higher the speed of circuit and vice versa. The comprehensive delay analysis for conventional comparator and dynamic double tail comparator is presented in this paper. Post layout simulation results in 0.18 um CMOS technology showed that the delay is reduced as compared to the conventional comparator. The analysis shows the suitability of the double tail comparator design for high speed ADCs like flash ADC which is used in portable devices.

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