International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 03 Issue: 04 | Apr-2016 www.irjet.net p-ISSN: 2395-0072

Verification of 8x10 Encoder and 10x8 Decoder with 3-bit down Ripple Counter for USB 3.0 Applications

P. Naveen Kalyan [1], K. Jaya Swaroop [2]

[1]*Student, Department of ECE, QIS College Of Engineering , Andhra Pradesh, INDIA*

[2]*Assistant Professor, Department of ECE , GISTcollege , Andhra Pradesh, INDIA*

Abstract - *The design and the implementation of* 8x10 *encoder and* 10x8 *decoder by using 3 bit down ripple counter Has been proposed in this paper .In a ripple counter , a flip-flop output transition serves as source for triggering other flip-flops .The clock skew problem can be reduced by using this ripple counter technique. By reducing clocks skew we can reduce the power consumption of hardware. So ripple counter technique has been used in this paper for the purpose of reducing the power consumption of the encoder and decoder circuits .The RTL schematic of* 8x10*encoder with ripple counter is shown in fig 9 and the fig 10 shows the RTL schematic* 10x8 *decoder with ripple counter .The clock power of an encoder circuit is reduced by11.11% at a frequency of 20mhz and the chip power of an encoder is reduced by 2.70% both the clock power and on chip power of decoder circuit are reduced 8.33% and 0% respectively at same frequency .The clock power and on the chip power of decoder is reduced to 10.17%and 22.15%at a frequency range of 200 MHz .Similarly the clock power and on chip power of a decoder are reduced to 7.44% and 4.33% at the same frequency. By using verilog HDL designing of 3 circuits i.e.....* 8x10 *encoder* 10x8 *decoder and 3 bit down ripple counter are done and the same are simulated in model sim 10.3. Xilinx ISE suit 13.4 has been used for the purpose of RTL, technology schematics and power report of the implemented circuit. By using FPGA of kintex 7 family the verification of encoder and decoder with ripple counter has been done* **.**

Key Words: *Xilinx; Verilog; ModelSim;8x10 encoder and 10x8 decoder*

1.INTRODUCTION

The VLSI engineers gives more emphasis on the resources used by the hardware. They are trying hard to reduce the consumption of resources which leads to the growth of the VLSI industry. The main resource comes into role is power. Less power consumption will certainly leads to less cost of the hardware. Lot of research is going on reduction of power consumed by the hardware

There are many techniques which are used to reduce the power such as clock gating and clock divider etc These techniques can also be used to reduce the clock skew problem and due to removal of clock skew power consumption can be reduced. USB 3.0 adds the new transfer rate referred to as SuperSpeed USB (SS) that can transfer data at up to 5 Gbit/s (625 MB/s), which is about ten times as fast as the USB 2.0 standard. Manufacturers are recommended to distinguish USB 3.0 connectors from their USB 2.0 counterparts by blue color-coding of the Standard-A receptacles and plugs, and by the initials SS. In USB 3.0, dual-bus architecture is used to allow both USB 2.0 (Full Speed, Low Speed, or High Speed) and USB 3.0 (Super Speed) operations to take place simultaneously, thus providing backward compatibility. Connections are such that they also permit forward compatibility, that is, running USB 3.0 devices on USB 2.0 ports. The structural topology is the same, consisting of a tiered star topology with a root hub at level 0 and hubs at lower levels to provide bus connectivity to devices

In this paper, we have designed the 8x10 encoder and 10x8 decoder using Verilog HDL. The encoder and decoder is implemented with 3-bit down ripple counter to improve the clock skew which certainly leads to less power consumption of encoder and decoder. The 8x10 encoder and 10x8 decoder have mainly two features due to which they are in great demand for high speed communication. First is low transmission rate and second is DC compensation . They have many applications such as PCI express, USB 3.0, gigabit ethernet and many more.

2. ARCHITECTURE

In this paper, we implemented 3-bit down ripple counter which is one of the techniques to reduce the clock skew problem. By reducing the clock skew we can able to reduce the power consumption of the hardware. We implemented this ripple counter with the encoder and decoder design using verilog HDL. There are many ways to implement the ripple counter depending on the characteristics of the flip flops used and the requirements of the count sequenceThe working of encoder, decoder and ripple counter design is illustrated later in this section.

The clock ports of the encoder and decoder block are driven by the output of the last flip-flop of the 3-bit ripple counter. By using ripple counter the consumed power of encoder is

reduced. The connection between the encoder and ripple counter block is more understand by the RTL view shown in Fig.----- and the connection between the decoder and ripple counter block is shown by the RTL view in Fig.----

3. Ripple Counter

A ripple counter is an asynchronous counter where only the first flip-flop is clocked by an external clock. All subsequent flip-flops are clocked by the output of the preceding flip-flop. Asynchronous counters are also called ripple-counters because of the way the clock pulse ripples it way through the flip-flopsIn the ripple counter design, the succeeding flip flop clock port is driven by the previous flip flop output port as shown in Fig.1. The clock skew is reduced by this because the flip flops don't toggle on the same clock. The first flip flop is clocked on the positive edge of the CLK signal and the second and the third stage flip flops are clocked on the positive edge of the output of the previous flip flop

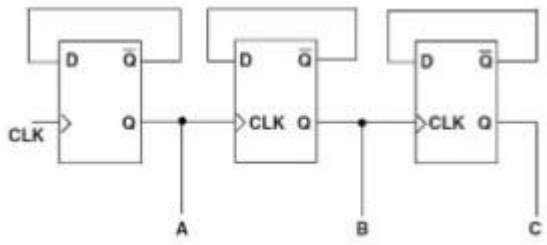

Fig-1: 3-bit Down Ripple Counter

3.1 8x10 Encoder and 10x8 Decoder

In the 8x10 encoder design, there are 8 inputs (ABCDEFGH) and these inputs are encoded into 10 outputs (abcdeifghj). For encoding the inputs, two different encoding schemes are used. One is 5 bits to 6 bits encoding and second is 3 bits to 4 bits encoding. Detailed working is referred in the literature

In the 10x8 decoder design, there are 10 inputs (abcdeifghj) and these inputs are decoded into 8 outputs (ABCDEFGH). For decoding the inputs, two different decoding schemes are used. One is 6 bits to 5 bits encoding and second is 4 bits to 3 bits encoding. Detailed working is referred in the literature

4. Simulation Result

The 8x10 encoder, 10x8decoder and ripple counter circuit are implemented using verilog HDL and stimulated on ModelSim 10.3c. The RTL and the technology view of the encoder with ripple counter and decoder with ripple counter is done in Xilinx ISE 13.4.

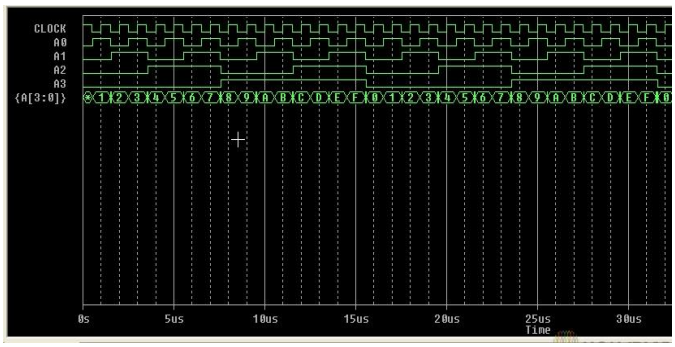

Fig-2: Demonstrations the stimulation waveforms of the 3bit down ripple counter

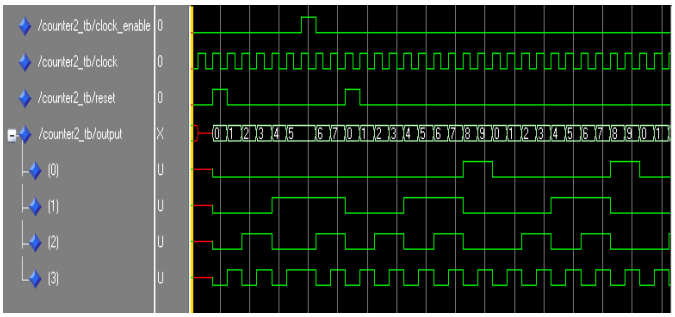

Fig-3: Stimulation Output of 3-bit Down Ripple counter

The 8x10 encoder with ripple counter circuit is shown in Figs.4. In these figures the encoder clock port is driven by the output of the ripple counter

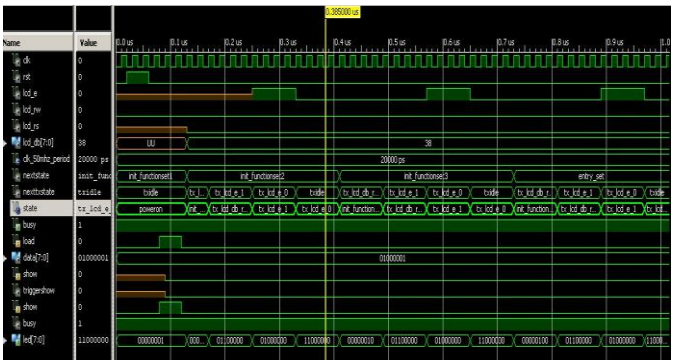

Fig-4: Simulation Output of 8x10 Encoder with Ripple Counter

The 10x8 decoder with ripple counter circuit is shown in Figs.6, 7, 8. In these figures the decoder clock port is driven by the output of the ripple counter.

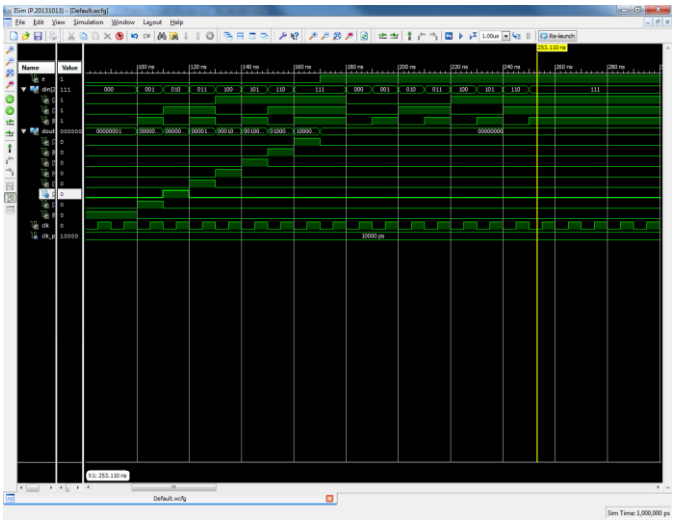

Fig.5: Simulation Output of 10x8 Decoder with Ripple Counter

5. CONCLUSIONS

In this paper we calculated the power of 8x10 encoder and 10x8 decoder. We compare the powers of encoder and decoder with the power obtained by 8x10 encoder with ripple counter and 10x8 decoder with ripple counter. Using 3-bit ripple counter in the encoder decoder circuit consumes less power and also avoids the problem of clock skew. The 8x10 encoder with ripple counter and 10x8 decoder with ripple counter are verified in FPGA of Kintex 7 family. These powers are calculated by using Xilinx XpowerAnalyser of Xilinx ISE suite 13.4.

The comparison of the powers between 8x10 encoder and 8x10 encoder with ripple counter is shown in Table 1

Table.1: Comparison of Encoder Powers

Powers (mW)		Frequency (MHz)	
		20	*200*
Encoder	*Clock Power*	0.18	1.77
	On-chip Power	111	149
Encoder with Ripple Counter	*Clock Power*	0.16	1.59
	On-chip Power	108	116

The comparison of the powers between 10x8 decoder and 10x8 decoder with ripple counter is shown in Table 2

Table.2: Comparison of Decoder Powers.

Powers (mW)		Frequency (MHz)	
		20	*200*
Decoder	*Clock Power*	0.12	1.21
	On-chip Power	108	116
Decoder with Ripple Counter	*Clock Power*	0.11	1.12
	On-chip Power	108	111

From the Table I and Table II, we come to a conclusion that the power consumption of encoder and decoder circuit is reduced by using ripple counter. Ripple counter also reduce the clock skew problem which improves the speed of the circuit. In this paper, we used two different frequencies for the analysis of encoder and decoder circuit as shown in theTable I and Table II. At 20 MHz frequency, the clock power of encoder circuit is reduced by 11.11% and the on-chip power of encoder circuit is reduced by 2.70%. For the same frequency the clock power and on-chip power of decoder circuit is reduced by 8.33% and 0% respectively. At 200 MHz frequency, the clock power of encoder circuit is reduced by 10.17% and the on-chip power id reduced by 22.15%. For the same frequency the clock power and on-chip power of decoder circuit is reduced by 7.44% and 4.31% respectively.

REFERENCES

[1] A.X.Widmer, P.A.Franaszek, "A DC-Balanced Partitioned-Block, 8B/10B Transmission Code," IBM J.RES. DEVELOP Vol.27, No.5, and September 1983.

[2] JagritKathuria, M. Ayoubkhan, Arti Noor, "A Review Of clock Gating Technique," MIT International Journal of Electronics and Communication Engineering, MIT Publications, ISSN 2230-7672, Vol 1, No.2, Aug 2011.

[3] Gajendra Singh Solanki, Rekha Agarwal, Sandhya Sharma, "Power Optimization of High Speed Pipelined 8B/10B encoder," International Journal of Innovative Technology & Exploring Engineering, Vol.3, No.7, December 2013.

[4] Mohammad Maadi, "An 8b/10b Encoding Serializer/Deserializer (SerDes) Circuit For High Speed Communication Application Using a DC Balanced, Partitioned Block, 8B/10B Transmission Code," International Journal of Electronics & Electrical Engineering, Vol.24, No.2, April 2014.

[5] KanikaSahni, KiranRawat and Sujata Pandey, "Power Optimization of 8b/10b Encoder Decoder Used For High Speed Communication," Industrial and Information Systems (ICIIS), 2014 9th International Conference on15-17 Dec. 2014.

[6] KanikaSahni, KiranRawat and Sujata Pandey, "A Low Power Approach for Implementation of 8B/10B Encoder and 10B/8B Decoder Used for High in a decoder Speed Communication,"Emerging Technology Trends in Electronics, Communication and Networking (ET2ECN), 2014 2nd International Conference on 26-27 Dec. 2014.