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A Survey of Various Metaheuristic Algorithms Used to Solve VLSI Floorplanning Problem

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Abstract - *Floorplanning is an important problem in very large scale integrated-circuit (VLSI) design automation as it determines the performance, size, yield, and reliability of VLSI chips. From the computational point of view, VLSI floorplanning is an NP-hard problem. Modern very large scale integration technology is based on fixed-outline floorplan constraints, generally with an objective of minimizing area and wirelength between the modules. This survey paper gives an up-to-date account on various metaheuristic algorithms used to solve VLSI floorplanning problem.*

Key Words: **Metaheuristic Algorithms, Slicing Floorplan, Soft Modules, Hard Modules, Simulated Annealing, VLSI Floorplanning**.

1. INTRODUCTION

As technology advances, circuit sizes and design complexity in modern VLSI design are increasing rapidly. To handle the design complexity, hierarchical design and reuse of IP modules become popular, which makes floorplanning or placement much more important than ever [1]. A floorplan is a rectangular dissection which describes the relative placement of electronic modules on the chip. The exponential increase in the size of digital circuit, reduction in chip size and heterogeneity of circuit elements used in modern chips lead to an increase in the complexity of modern digital circuit layout and design of algorithms [2]. The development of integration technology has followed the famous Moore's Law [3].Gordon Moore, the co-founder of Intel, in the year 1965, stated that "The number of transistors per chip would grow exponentially (double every 18 months)". In the design of VLSI (Very Large-Scale Integrated) circuit's floorplanning is an important phase. It determines the topology of layout and this problem is known to be NP-hard (Non-deterministic Polynomial-time hard) and it has received much attention in recent years**.** The solution space of the problem will increase exponentially with the growth of circuits scale, thus it is impossible to find the optimal solution by exploring the global solution space [4].

The digital circuit layout problem is a constrained optimization problem in the combinatorial sense. It is an important part of the digital circuit design process. For a circuit represented by net list, a set of modules, its dimensions and a set of pins, the layout problem seeks an assignment of geometric coordinates of the circuit components fulfilling the requirements of the fabrication technology (sufficient wire spacing, restricted number of wiring layers etc.) while minimizing certain cost criteria. This is accomplished in several stages such as partitioning, floorplanning, placement and routing with each step being a constrained optimization problem [5]. Floorplanning is an essential design step in physical design of VLSI circuits to plan the positions of a set of circuit modules on a chip in order to optimize the circuit performance. The major objective of floorplanning is to allocate the modules of a circuit into a chip to optimize some design metric such as area, wire length and timing. During floorplanning the designers have additional flexibility in terms of size shape and orientation of the modules on chip. The shape of the chip and that of the modules is usually a rectangle. The representation has a great impact on the feasibility and complexity of floorplan designs. In this paper details about various aspects of floorplan design problem is given along with the complete literature survey of VLSI floorplanning problem.

2. VLSI FLOORPLAN DESIGN PROBLEM

2.1 Problem Description

Very large-scale integrated floorplan is to arrange the modules on a chip and the given inputs of the placement problem is a set of blocks defined as B = {B1, B2, ….Bn}. Each block Bi is rectangular with fixed orientation and a tuple (wi, hi), where wi is defined as the width and hi is defined as the height. There are two different types of modules:

1. Hard module. The hard module's shape is fixed, and is denoted as (W, H), where W is the width and H is the height of the module.
2. Soft module. Soft module's area is also fixed, but the ratio of width/height is included in a given range. It can be denoted as (S, L, U), where S represents the area, L and U the lower and upper boundary of the width/height ratio. In case that the modules are given, the objective of VLSI floorplanning is to arrange the modules on a chip under the constraints that any two modules are not overlapped, and the area, wire length and other performance indices are optimal [4].

2.2 Floorplan Structure

There are two layout structures in floorplan, namely, slicing and non-slicing floorplan. A slicing floorplan can be obtained by repetitively cutting the floorplan horizontally or vertically, whereas a non-slicing floorplan cannot [6]. The given dimension of each hard module must be kept. All modules are free of rotation; if a module is rotated, its width and height are exchanged. Figure 1 shows a slicing floorplan. A slicing tree is used to represent a slicing floorplan; it is a binary tree with modules at the leaves and cut types at the internal nodes. There are two cut types, H and V. The H cut divides the floorplan horizontally, and the left (right) child represents the bottom (top) sub-floorplan. In Similar way, the V cut divides the floorplan vertically, and the left (right) child represents the left (right) sub-floorplan.

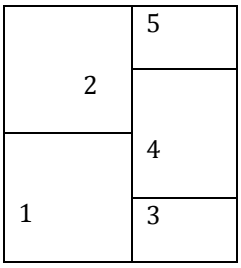

Fig 1. Slicing floorplan

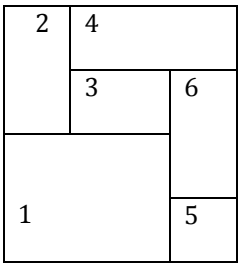

Fig 2. Non-Slicing floorplan

The non-slicing floorplan is more general than the slicing floorplan as shown in Figure 2. However, because of its non-slicing structure, slicing tree cannot be used to model it. Instead, we can use a horizontal constraint graph (HCG) and a vertical constraint graph (VCG) to model a non-slicing floorplan.

2.3. Floorplan Representation

To apply any optimization approach for floorplan design, we need to first encode a floorplan as a solution which is called a floorplan representation. A floorplan representation not only induces a solution space that contains all feasible solutions defined by the representation but also induces a unique solution structure that guides the search of the optimization approach to find a desired floorplan in the solution space. Most popular floorplan representations are Normalized Polish Expression, B*-tree, Sequence Pair, O-tree. Details about various floorplan representations that have been used for VLSI floorplanning can be seen in [7].

2.4 Floorplanning Cost

The goal of floorplanning is to optimize a predefined cost function, such as the area of a resulting floorplan given by the minimum bounding rectangle of the floorplan region. Chip silicon cost directly correlates to the floorplan area. Chip silicon cost will be high if the area is large. The space in the floorplan bounding rectangle uncovered by any module is called white space or dead space. Other floorplanning cost, such as wirelength, will also be considered. Shorter wirelength not only can reduce signal delay but also can facilitate wire interconnection at the routing stage. So the objective of floorplanning can also be a combined cost, a combination of area plus wirelength.

3. MODERN FLOORPLANNING CONSIDERATIONS

Increasing design complexity and new circuit properties and requirements have reshaped the modern floorplanning problem. The new considerations and challenges make the problem much more difficult. Two such crucial considerations are following:-

3.1 Soft Modules

Unlike hard modules with fixed heights and widths, soft modules can change their heights and widths while keeping the same module area. The aspect ratio bounds are given as inputs for each module. There are many techniques for the adjustment of soft-module dimensions.

3.2 Fixed-outline Constraint

Modern VLSI design is typically based on a fixed-die (fixed-outline) floorplan [8], rather than a variable-die floorplan. A floorplan with pure area minimization without any fixed-outline constraints may be useless, because it cannot fit into the given outline. The classical floorplanning usually handles only module packing to minimize silicon area, unlike it the modern floorplanning should be formulated as fixed-outline floorplanning.

4. LITERATURE REVIEW ON VARIOUS METAHEURISTIC ALGORITHMS

In the context of circuit design, floorplanning is the process of placing circuit modules of arbitrary sizes and dimensions on a given layout area with an objective of minimizing area and wirelength between the modules and this problem has been solved by using various iterative approaches in literature [9]. They search for an improved floorplan by making local changes until a feasible floorplan is gained or no more improvements can be obtained. A detailed literature review of the popular metaheuristic algorithms that have been used to address VLSI floorplanning problem is given below.

4.1 Simulated Annealing (SA)

It is one of the most popular methods for floorplan optimization. To apply simulated annealing for floorplan design, firstly floorplan is encoded as a solution, called a floorplan representation, which models the geometric relation of modules in a floorplan. This floorplan representation not only induces a solution space that contains all feasible solutions defined by the representation but also induces a unique solution structure that guides the search of simulated annealing to find a desired floorplan in the solution space ([10], [11]).

D. F. Wong and C. L. Liu (1989) [12] used polish expressions to represent floorplans and employ the search method of simulated annealing. They used simulated annealing for the case where all modules are rectangular and minimize area and interconnection wirelength.

Koji kiyota, Kunihiro fuiiyoshi (2000) [13] proposed a novel solution space of floorplans for simulated annealing (SA) which consists of the all general floorplans with exact n rooms, where n is the number of given modules, using sequence pair.

Chen, T.C., Chang (2006) [14] have studied two types of modern floorplanning problems: 1) fixed-outline floorplanning and 2) bus-driven floorplanning (BDF). This floor planner uses B*- tree floorplan representation based on fast three-stage simulated annealing (SA) scheme called Fast-SA.

Fang, J.P., Chang, Y.L, *et. al.* (2009) [15] adopted a parallel computing environment to increase the throughput of solution space searching in order to deal with the floorplan design with enormous amount of interconnections and design blocks.

S. Anand , S. Saravanasankar (2010) [16] the aim of their work was to minimize the unused area, that is, dead space in the floorplan, in addition to these objectives. They developed a Simulated Annealing Algorithm (SAA) based heuristic, namely Simulated Spheroidizing Annealing Algorithm (SSAA) and improvements in the proposed heuristic algorithm are also suggested to improve its performance.

Jianli Chen, Wenxing Zhu **(**2011) [17] presented a hybrid simulated annealing algorithm (HSA) for nonslicing VLSI floorplanning. They used a new greedy method to construct an initial B*-tree, a new operation on the B*-tree to explore the search space.

4.2 Genetic Algorithm (GA)

It is a global search technique inspired by evolution. The crux of GA lies in the "survival of the fittest" strategy. The input to GA is a set of random individuals, termed as the initial population. Each individual in the population is a chromosome that represents a solution to the given problem in an encoded form. Using well-defined genetic operators, GA evolves the individuals in the population generation by generation until an optimal or near to optimal solution is found. The fitness of the individuals is evaluated in a fitness function.

B. Gwee and M. Lim (1999) [18] described a genetic algorithm with heuristic-based layout decoder (GAHD) for floorplanning in IC design which use GA to search for an optimal arrangement of circuit modules on a pre-specified layout area.

Ning Xu, Feng Huang *et. al.* (2006) [19] proposed a multithread scheme for parallelizing a genetic algorithm for BBL placement optimization. The parallel genetic algorithms (PGA) are realized, using sequence-pair (SP) as the representation in order to either speed up a problem or to achieve a higher accuracy of solutions to a problem.

Maolin Tang and Xin Yao (2007) [20] proposed a memetic algorithm (MA) for a nonslicing and hard-module VLSI floorplanning problem. This MA is a hybrid genetic algorithm

that uses an effective genetic search method to explore the search space and an efficient local search method to exploit information in the search region.

Pradeep Fernando and Srinivas Katkoori (2008) [21] proposed a multi-objective genetic algorithm for floorplanning that simultaneously minimizes area and total wirelength. The proposed genetic floor planner is the first to use non-domination concepts to rank solutions. Samsuddin *et. al.* (2008) [22] proposes an optimization approach for macro-cell placement which minimizes the chip area size. The binary tree method for non-slicing tree construction process is utilized for the placement and area optimization of macro-cell layout in very large scaled integrated (VLSI) design. Various types of genetic algorithms: simple genetic algorithm (SGA), steady-state algorithm (SSGA) and adaptive genetic algorithm (AGA) are employed in order to examine their performances in converging to their global minimums.

Jianli Chen, Wenxing Zhu (2010) [23] described that hybrid genetic algorithm (HGA) uses an effective genetic search method to explore the search space and an efficient local search method to exploit information in the search region.

Gracia Nirmala Rani, Rajaram.S *et. al.* (2012) [24] presented a Genetic (GA) algorithm based thermal-aware floorplanning framework. Primary objective for floorplanning is to minimize the total area required to accommodate all of the functional blocks on a chip and also to reduce high temperature and to distribute temperature evenly across a chip in an framework. B*tree representations with Genetic (GA) algorithm is used to calculate floorplanning temperature based on the power dissipation.

4.3 Particle Swarm Optimization (PSO)

It is an optimization technique inspired by swarm intelligence and theory in general such as bird flocking and even human social behavior. PSO is a population-based evolutionary algorithm in which the algorithm is initialized with a population of random solutions. However, unlike most of other population-based evolutionary algorithms, Particle swarm optimization is motivated by the simulation of social behavior instead of the survival of the fitness.

Guolong Chen *et. al.* (2008) [25] proposed a novel floorplanning algorithm based on Discrete PSO (DPSO) algorithm, in which integer coding based on module number was adopted and the principles of mutation and crossover operator in the Genetic Algorithm (GA) are also incorporated into the proposed PSO algorithm to achieve better diversity and break away from local optima.

Zhen Chen *et. al.* (2012) [26] proposed a co evolutionary multi objective particle swarm optimization (CMOPSO) algorithm to solve a VLSI Floorplanning problem which is a multi-objective combinatorial optimization and has been proved to be a NP-hard problem.

4.4 Ant Colony Optimization

Ant colony optimization (ACO) is a population based metaheuristic that can be used to find optimal solution to difficult optimization problems. One of the most intensively studied problems in the area of optimization is travelling salesman problem (TSP). The travelling salesman problem is a problem in combinational optimization. It is a NP-hard problem.

The ant-based metaheuristic algorithm consists of three stages, which are the initialization, the construction and the feedback. The primary stage i.e. initialization stage involves the parameters settings such as the number of colonies and the number of ants. The next stage i.e. construction stage involves the construction of path on the basis of pheromone concentration. The last one i.e. the feedback stage deals with the extraction and the reinforcement of the ants travelling experiences obtained during the previous searching path.

Chyi-Shiang Hoo *et. al.* (2013) [27] proposed a new floorplanner, namely Variable-Order Ant System (VOAS) is proposed to handle VLSI floorplanning design. VOAS transforms parameter ˇ in Ant System (AS) to a variable and these varying local and global factors enable the ant to make the best possible choice. Experimental results by using MCNC and GSRC benchmark circuits show that VOAS gives improved results in terms of area and composited function of area and wire length, as compared to other state-of-the-art and recent floorplanning/placement algorithms.

5. CONCLUSION

In the context of circuit design, floorplanning is the process of placing circuit modules of arbitrary sizes and dimensions on a given layout area and it gives answer to the different questions of VLSI design such as shape of modules and location of modules. The major objective of floorplanning is to allocate the modules of a circuit into a chip to optimize some design metric such as area, wire length and timing. Optimized VLSI floorplan designs will improve the performance and size of VLSI chips. It will also be helpful in determining the yield and reliability of VLSI chips.

6. FUTURE SCOPE

For modern floorplan designs, another extension can be to work with rectilinear modules (for instance, T-shaped or L-

shaped modules). That can be done by splitting these rectilinear shapes into rectangles and modifying the placing algorithm to keep those corresponding rectangles compacted. As technology advances, the number of modules in a chip becomes large, so to cope with the scalability problem effectively and efficiently, hierarchical floorplanning can also be used. The hierarchical approach recursively divides a floorplan region into a set of sub-regions and solves those sub-problems independently.

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