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FPGA based Efficient Routing Implementation of programmable Network on chip

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Abstract - *A large no complex system on chips are getting developed as a result of increase in chip density following Moore's law. The advanced So-Cs have in their self significantly noticeable communication mechanisms. No-C have solved the scalability problems to a larger extent as compared to bus based interconnect. No-C has been providing a back bone architecture for System-on-chips since long. Among the available communication matrices No-C has helped tremendously in the communication performance enhancement. No-C research majorly involves work on packet switching, though at the same time circuit switching assures high communication rates and predictable communication latencies. The current research is mainly focusing towards implementation of No-C architecture for FPGA based designs using circuit switching approach. Proposed implementation has enhancement of light weight circuit switched architecture. The programmable No-C architecture is implemented using VHDL and synthesized on the Virtex-5 XC5VLX20T package FF323 device at 139 M-Hz. It provides sufficient customization on the number of ports, nodes and amount of data. Validation of performance improvement over the existing implementation has been done by experimental synthesized results.*

Key Words: No-cs, FPGA, So-cs, Asynchronous , GALS.

1.INTRODUCTION

The implementation of very large systems on a single chip is termed as System on chip (SoC). These architectures generally consist of combination of CPUs, memories and custom hardware models. SoCs could also be put into practice on Programmable Logic Devices (PLDs), e.g. Field Programmable Gate Arrays (FPGA) or Complex Programmable Logic Device (CPLD).The immediate need of programmable SoCs have made significant contribution in on chip system world because of two major reasons mentioned under:

[1] The bus based communication creates scalability issues with increasing system complexity and could prove to be an important bottleneck, thus giving rise to the adoption of Network on chip architecture. NoCs have successfully addressed the problem of SoC scalability. The concept of programmability among NoC has been taken into consideration by providing the architecture for the varied applications that are taking different shapes for different applications at various times.

[2]It also deals with design and verification, which plays a very important role in dealing with high level complexities .

FPGA based communication has become a very viable solution in this case, as design and verification could be repeated (n) number of times for any design idea within FPGA . A computing architecture for FPGAs has greatly simplified application development. It should absorbs away the differences between FPGA devices, while supporting communications with external devices at full interface speed, consuming as few resources as possible, and allowing the application to determine how data should be handled. FPGAs have been seen to be effective and efficient for performing a variety of computations . But at the same time due to the high non recurring engineering costs and long time to market for ASICs it is clearly been mentioned that more better use of FPGAs is been considered for designing different hardware applications . The state of the art FPGAs from Xilinx families, e.g. Spartan and Virtex consists of huge amount of resources that are essential for designing complex logic circuits, e. g. they have large number of configurable logic blocks (CLBs) and memory elements and hence sorts out the resource problems, occurred in traditional FPGAs.

1.1 Project Objective

[1]The advanced So-Cs have in their self significantly noticeable communication mechanisms. No-C has solved the scalability problems to a larger extent as compared to bus based interconnect.

[2] It provides good customization on the number of ports, nodes and amount of data.

[3] The work has been shown to be delivering better results in terms of clock frequency, which has shown improvisation compared to the earlier implementations.

[4] .Supports multiple topologies and options for various parts of the network -NoC interconnect supports use of different optimizations and topologies for different parts of the network. For example, a design may have a set of high-frequency, high throughput components, such as processor.

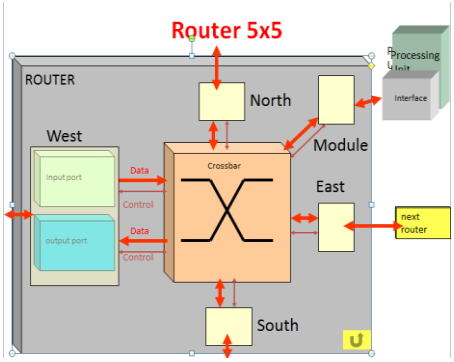
1.2 Literature Review

[1] A-DfT Architecture for Asynchronous Networks-on-Chip.HAL This paper is published by Xuan Tu Tran, Jean Durupt, Fran¸cois Bertrand in MAY 2006, they studied on the bases of The Networks-on-Chip (NoCs) paradigm is emerging solution for the communication of SoCs. Many NoC architecture propositions are presented but few works on testing these network architectures.

[2] Efficient Routing Implementation of Programmable Network on Chip on FPGA using Circuit Switching Appro This paper is published by Parag Parandkar , Purnima Khandelwal , Geetesh Kwatra in Volume 5, Issue 1, January 2015, the study made by them was Advanced SoCs have in their shelf significantly noticeable communication mechanisms. NoC has solved the scalability problems to a larger extent compared to bus based interconnect. NoC has been providing a back bone infrastructure for System-on-chips since long .

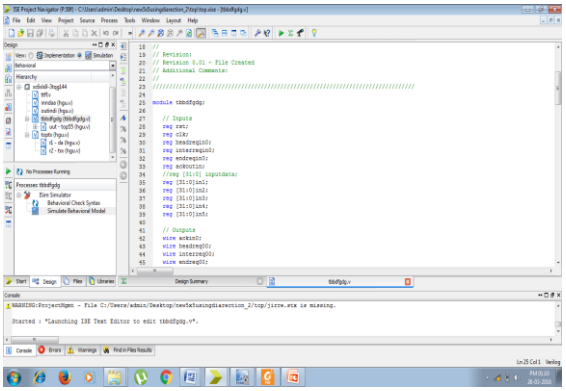
[3] P-NoC: a flexible circuit-switched No-C for FPGA-based systems This paper was published by C. Hilton and B. Nelson in 31st October 2005 and revised in 8th February 2006 they studied on the bases of Such So-Cs can also be implemented on FPGA substrates, something we will refer to as programmable So-Cs (P-SoCs), in this paper.

1.3 Block Diagram and Discription

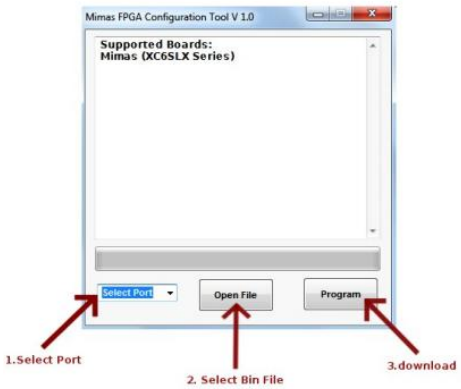


The router has five bidirectional interfaces where four of them are connected to the neighbor routers , and each router has a direction. There are four directions north, south, east, west and through this the physical links and the fifth one is connected to the IP core through the Network Adapter (NA).The router is designed such that when a flit enters the router it can only be routed to the output ports of the others four interfaces and cannot be routed back in the same direction. The routing direction is encoded in the header flits using the two MSB . The connection between the input and output ports is established through a non-blocking crossbar and hence the router can accept any number of simultaneous inputs.

1.4 Software Development



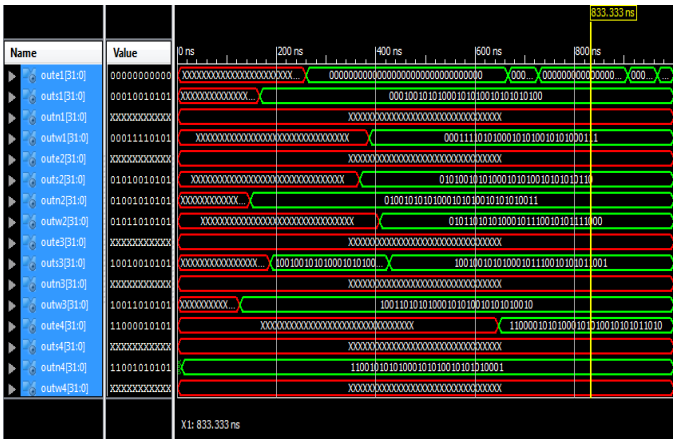
[1]The above snapshot show the xilinx design suite 4.2 software which is used for simulation of vlsi codes. Here verilog language is used , it's a mixture of VHDL and c programming .It is also used to burn the program on the spartan6 module.



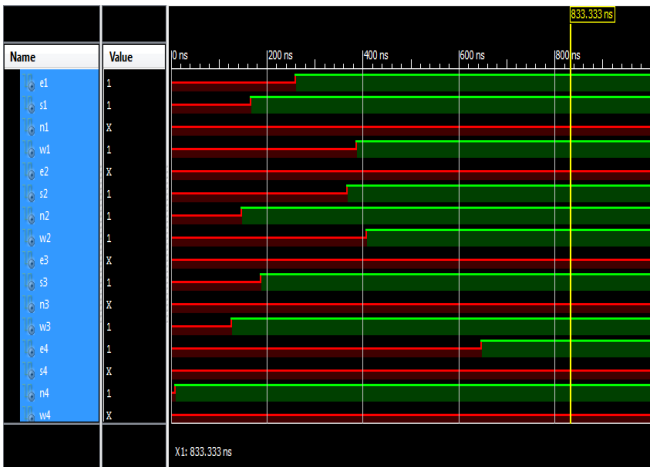
[2]The above snapshot shows configuring Mimas. Open Mimas Configuration Tool. Select the port no.

[3]Above snapshot shows that the program is fed to the spartan6 module kit.

2.RESULT



[1]The above snapshot shows that we are sending 4 inputs through fours ports in binary format. It shows the simulated window, and we use xilinx design suite 14.2 to get the simulated output .



[2]the above snapshot shows the simulated window of the output port .There are 4 output ports

3. CONCLUSION

Basically this system focuses on light weight circuit switched approach is depicted for FPGA based systems. The project has been shown to be delivering better results in terms of clock frequency improvisation compared to the earlier implementations. The programmable No-c architecture is being implemented using Mimas Spartan6 FPGA Module. It is basically a n*n router where the inputs can be customized and can be decreased or increased. Validation of performance improvement has been implemented by experimental synthesis result. Due to this the current design is further modified and enhances using higher leve hardware languages working on system level Hardware languages working on system level like that of system C and system Verilog.

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