Video Graphics Array interfacing through Artix-7 FPGA

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Abstract - *This paper presents the design of VGA controller and it is used to establish an interconnection between a LCD screen[8][7] and Artix-7[4] FPGA kit through VGA port to display various colours on the LCD Monitor. The board will be a Digilent Nexys4 DDR Artix-7 [6]FPGA Board. The Nexys4 DDR board[3] is a complete, ready-to-use digital circuit development platform based on the latest Artix-7 Field Programmable Gate Array (FPGA) from Xilinx. With its large, high-capacity FPGA (XC7A100T-1CSG324C), 16 user switches, 12-bit VGA output. The Artix-7 FPGA is optimized for high performance logic, and offers more capacity, higher performance, and more resources than earlier designs.*

The Nexys4 DDR board uses 14 FPGA signals to create a VGA port with 4 bits-per-color and the two standard sync signals (HS – Horizontal Sync, and VS – Vertical Sync).This design has achieved 4096 different colors can be displayed, one for each unique 12-bit pattern.14-bit VGA controller [1]design Intellectual Property (IP) core is built by developing using Verilog HDL with relevant tools such as Model Sim, Xilinx Vivado Design suite (ver:15.1), which provides a fast and easy interface to LCD screen.

Keywords:VGA,ARTIX7,FPGA,IP,VSYNC,HSYNC,VIVADO,VERILOG,RGB,XDC,TDISP

1. Introduction

VGA[10] is a high-resolution video standard[11] used mostly for computer monitors, where ability to transmit a sharp, detailed image is essential. VGA uses separate wires to transmit the three color component signals and vertical and horizontal synchronization signals.

1.1 Video Graphics Array

The term Video Graphics Array (VGA) refers either to an analog computer display standard, the 15-pin D-sub miniature VGA connector[9], or the 640×480 resolution itself.

The VGA specifications are as follows:

- 256 KB Video RAM
- 16-color and 256-color modes
- 262144-value color palette (six bits each for red, green, and blue)
- Selectable 25.2 MHz or 28.3 MHz master clock
- Maximum of 720 horizontal pixels
- Maximum of 480 lines
- Refresh rates at up to 70 Hz
- Vertical Blanking interrupt (Not all cards support this.)
- Planar mode: up to 16 colors (4 bit planes)
- Packed-pixel mode: 256 colors (Mode 13h)
- Hardware smooth scrolling support
- Some "Raster Ops" support
- Barrel shifter
- Split screen support
- 0.7 V peak-to-peak
- 75 ohm impedance (9.3mA - 6.5mW)

The VGA supports both All Points Addressable graphics modes, and alphanumeric text modes. Standard graphics modes are:

- 640×480 in 16 colors
- 640×350 in 16 colors
- 320×200 in 16 colors
- 320×200 in 256 colors

As well as the standard modes, VGA can be configured to emulate many of the modes of its predecessors (EGA, CGA, and MDA).

1.2 Requirements for VGA Display

- DB15 Connector
- VGA Display Port on the Artix-7 FPGA Kit
- Signal Timing for a 60Hz, 640X480 VGA Display

1.2.1 DB-15 Connector

DB-15 connector (male) & pin numbering appears as shown in Figure 1.

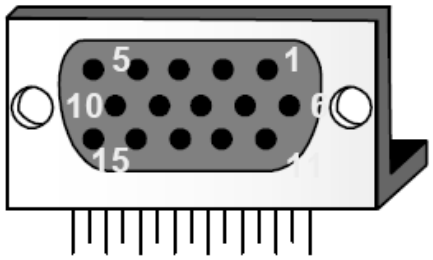


Fig 1: DB15 VGA Connector (front view)

Pin Description of VGA connector:

Table 1: Pin Description

PIN	SIGNAL NAME	DESCRIPTION
1	RED	Red video signal
2	GREEN	Green video signal
3	BLUE	Blue video signal
4	MONID(0)	Monitor ID signal 0
5	GND DDC	Return
6, 7, 8	AGND_VID	Analog video ground
9	+5V_IO 5 V	Power for I/O device
10	GND	HSYNC and VSYNC ground
11	VGA_ID	VGA ID signal
12	MONID(2)	Monitor ID signal 2
13	HSYNC	Horizontal synchronization signal
14	VSYNC	Vertical synchronization signal
15	MONID(1)	Monitor ID signal 1

1.2.2 VGA Display Port on the Artix-7 FPGA Kit

The Nexys 4 DDR board[4] uses 14 FPGA signals to create a VGA port with 4 bits-per-color and the two standard sync signals (HS – Horizontal Sync, and VS – Vertical Sync). The color signals use resistor-divider circuits that work in conjunction with the 75-ohm termination resistance of the VGA display to create 16 signal levels each on the red, green, and blue VGA signals. This circuit, shown in Figure 11, produces video color signals that proceed in equal increments between 0V (fully off) and 0.7V (fully on). Using this circuit, 4096 different colors can be displayed, one for each unique 12-bit pattern. A video controller circuit must be created in the FPGA to drive the sync and color signals[12] with the correct timing in order to produce a working display system.

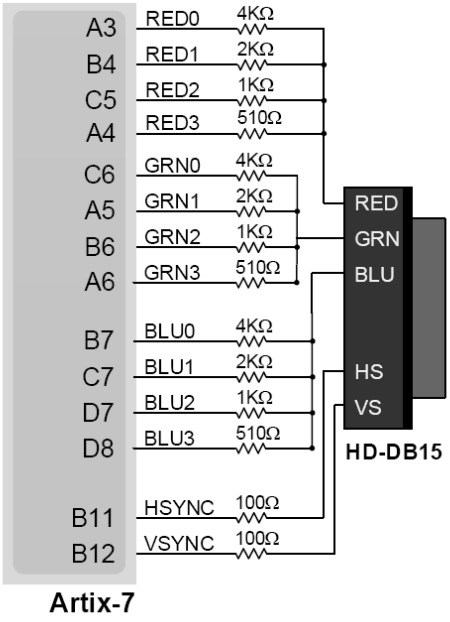


Fig 2: VGA Connections from Nexys4 DDR Board

The Artix-7 FPGA[4] directly drives the fourteen VGA signals via resistors. Each color line has a series resistor, with four bit each for RED,GREEN and BLUE. The line resistor, in parallel combinations with the 510Ω ,1kΩ,2kΩ,4kΩ and 100Ω termination built into the VGA cable, ensures that the color signals remain in the VGA-specified 0V to 0.7V range. The HSYNC and VSYNC signals using LVTTL or LVCMOS33 I/O standard drive levels. Drive the 4-bit RED, GREEN and BLUE signals high or low to generate the 4096 colors shown in Table2

1.2.3 Signal Timing for a 60Hz, 640X480 VGA Display

CRT-based VGA displays use amplitude-modulated, moving electron beams (or cathode rays) to display[12] information on a phosphor-coated screen. LCDs use an array of switches that can impose a voltage across a small amount of liquid crystal, thereby changing light permittivity through the crystal on a pixel-by-pixel basis. Although the following description is limited to CRT displays, LCDs have evolved to use the same signal timings as CRT displays. Consequently, the following discussion pertains to both CRTs and LCDs.

Table 2: 12-Bit Display Color Code(few combinations)

RED (4-bit)	GREEN (4-bit)	BLUE (4-bit)	Resulting Color
0000	0000	0000	Black
0000	0000	1111	Blue
0000	1111	0000	Green
0000	1111	1111	Cyan
1111	0000	0000	Red
1111	0000	1111	Magenta
1111	1111	0000	Yellow
1111	1111	1111	White

Within a CRT display[15], current waveforms pass through the coils to produce magnetic fields that deflect electron beams to transverse the display surface in a raster pattern, horizontally from left to right and vertically from top to bottom. As shown in Figure 3, information is only displayed when the beam is moving in the forward direction—left to right and top to bottom—and not during the time the beam returns back to the left or top edge of the display. Much of the potential display time is therefore lost in blanking periods when the beam is reset and stabilized to begin a new horizontal or vertical display pass.

The display resolution defines the size of the beams, the frequency at which the beam traces across the display and the frequency at which the electron beam is modulated. Modern VGA displays support multiple display resolutions and the VGA controller dictates the resolution by producing timing signals to control the raster patterns. The controller produces TTL-level synchronizing pulses[2] that set the frequency at which current flows through the deflection coils, and it ensures that pixel or video data is applied to the electron guns at the correct time.

Video data typically comes from a video refresh memory with one or more bytes assigned to each pixel location. The Artix-7 Nexys4 DDR [8]board uses 12-bits per pixel, producing one of the 4096 possible colors shown in Table 2. The controller indexes into the video data buffer as the beams move across the display. The controller then retrieves and applies video data to the display at precisely the time the electron beam is moving across a given pixel.

As shown in Figure 3, the VGA controller generates the horizontal sync (HS) and vertical sync (VS) timing signals and coordinates the delivery of video data on each pixel clock.

The pixel clock defines the time available to display one pixel of information. The VS signal defines the refresh frequency of the display or the frequency at which all information on the display is redrawn. The minimum refresh frequency is a function of the display's phosphor and electron beam intensity, with practical refresh frequencies in the 60 Hz to 120 Hz range. The number of horizontal lines displayed at a given refresh frequency defines the horizontal retrace frequency.

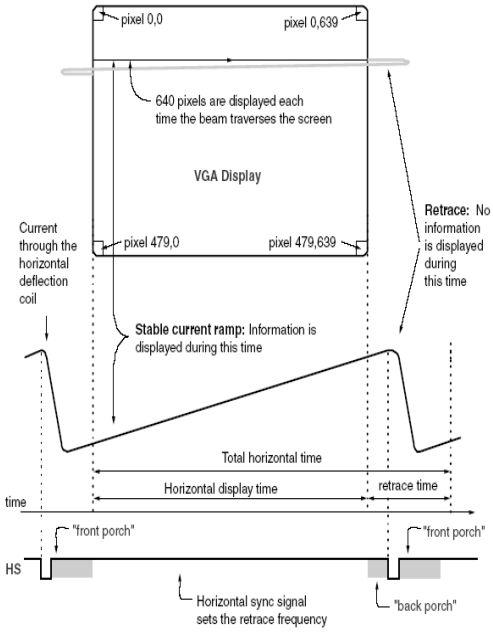


Fig 3: CRT Display Timing Example

2. Proposed VGA controller architecture

2.1 VGA Signal Timing

The signal timings in Table 3 are derived for a 640-pixel by 480-row display using a 25 MHz pixel clock and 60 Hz ± 1 refresh. Figure 5 shows the relation between each of the timing symbols. The timing for the sync pulse width (TPW) and front and back porch intervals (TFP and TBP) are based on observations from various VGA displays. The front and back porch intervals are the pre- and post-sync pulse times. Information cannot be displayed during these times.

Table 3: 640X480 Mode VGA Timing[2]

Symbol	Parameter	Vertical Sync			Horizontal Sync	
		Time	Clocks	Lines	Time	Clocks
T_S	Sync pulse time	16.7 ms	416,800	521	32 µs	800
T_{DISP}	Display time	15.36 ms	384,000	480	25.6 µs	640
T_{PW}	Pulse width	64 µs	1,600	2	3.84 µs	96
T_{FP}	Front porch	320 µs	8,000	10	640 ns	16
T_{BP}	Back porch	928 µs	23,200	29	1.92 µs	48

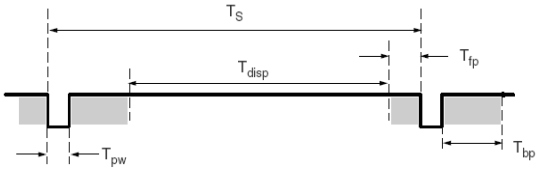


Fig 4: VGA Control Timing

Generally, a counter clocked by the pixel clock controls the horizontal timing. Decoded counter values generate the HS signal. This counter tracks the current pixel display location on a given row. A separate counter tracks the vertical timing. The vertical-sync[14] counter increments with each HS pulse and decoded values generate the VS signal. This counter tracks the current display row. These two continuously running counters form the address into a video display buffer. For example, the on-board DDR SDRAM provides an ideal display buffer.

Table 4: Timing Constraints for different Resolutions

Horizontal constants	Vertical constants
800X600 and 40 MHz Hactive <= "001100011111" HFP <= "001101000111" Hsynch <= "001111000111" Hin <= "001110000111" HBP <= "010000011111"	800X600 and 40 MHz Vactive <= "01001010111" VFP <= "01001011000" Vsynch <= "01001011100" VBP <= "01001110011"
1280x1024 @ 110MHz Hactive <= "010011111111" HFP <= "010100110011" Hsynch <= "010110101011" Hin <= "010101101111" HBP <= "011010101011"	1280x1024 @ 110MHz Vactive <= "01111111111" VFP <= "10000000010" Vsynch <= "10000000111" VBP <= "10000110001"

2.2 Block Diagram for VGA Display

The vgaController module to generate hSync, vSync, red(4-bit), green(4-bit), blue(4-bit) signals. The module takes in the 100MHz system clock on pin E3. The VGA timing should be based on the 60Hz refresh 640x480 VGA timing described in this handout. Implemented this module with Xilinx Vivado Design suite.

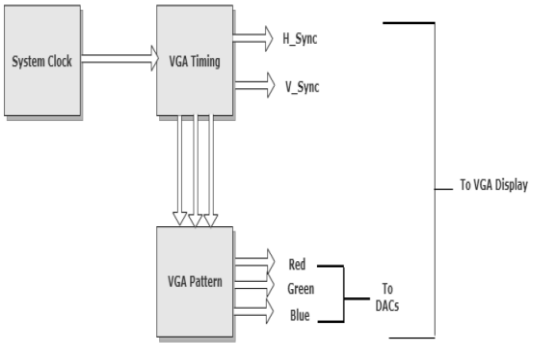


Fig 5: Block diagram for VGA Display

The top module is generated the outputs based on the 640x480 60Hz refresh timing in Figure 6. You can validate the timing by simulating the vgaController circuit in the Vivado simulator[3].

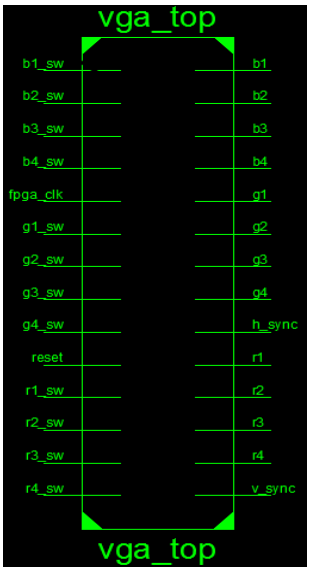


Fig 6: VGA Controller Top Module

The system clock on the Artix-7 board is 100MHz. By using 2-bit counter module system clock can be divided that by four and used that the output as the 25MHz clock. The hardware implementation shown in Figure 7.

Fig 7: FPGA Clock divider network

2.3 Flow Chart For VGA Display:

The following flowchart describes the operation of VGA controller IP core[2]. The steps involved in this algorithm are:

Step1: Reduce the FPGA clock frequency 100MHz to suitable for VGA clock frequency 25MHz.
Step2: Set H_Sync and V_Sync timing suitable for particular VGA mode.
Step3: Input RGB(12-bit) values to FPGA to get desired color on LCD monitor.
Step4: Increment x_pixels and y_pixels location.
Step5: Check the condition,

Is x_pixels==640 & y_pixels==480 ?

Condition is not match → increment both x_pixels and y_pixels for 640 and 480 repectively.
Condition is match → diplay the color on the LCD monitor

Step6: Stop the algorithm.

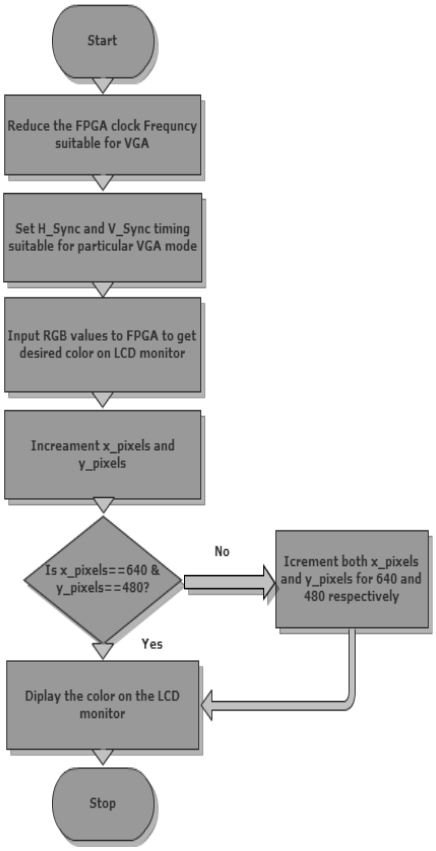


Fig 8: Flow chart for VGA display

3. FPGA Implementation Results

3.1 Synthesis results

The designed VGA controller[15] implemented on Artix7-FPGA using Xilinx Vivado design suite with the help of Xilinx design constraint (XDC) file[5] and also generated total power utilization report.

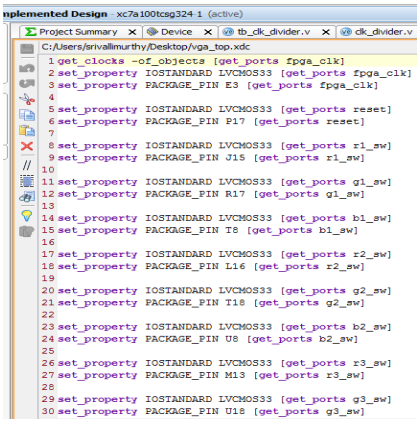


Fig 9: Xilinx Design Constraint (XDC) file.

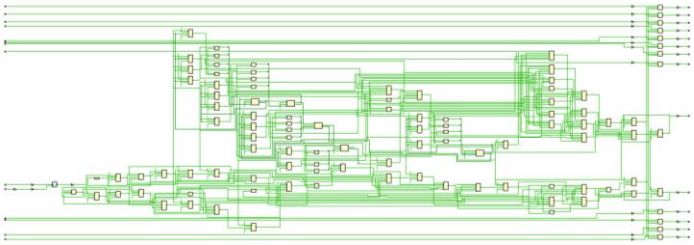


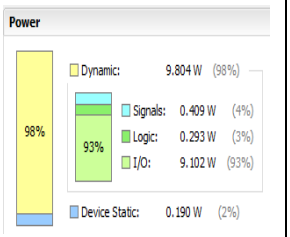
Fig 10 VGA Controller Schematic diagram

3.2 Power Analysis

Table 5: Artix-7 xc7a100tcsg323-1 FPGA Utilization and Power Analysis Report

Utilization - Post-Implementation

Resource	Utilization	Available	Utilization %
FF	35	126800	0.03
LUT	55	63400	0.09
I/O	28	210	13.33
BUFG	2	32	6.25



Power

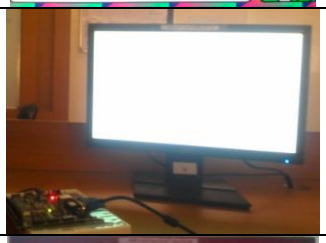
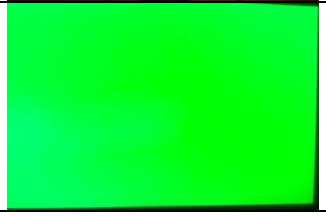
Total On-Chip Power:	**9.994 W**
Junction Temperature:	**70.6 °C**
Thermal Margin:	14.4 °C (3.1 W)
Effective ϑJA:	4.6 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

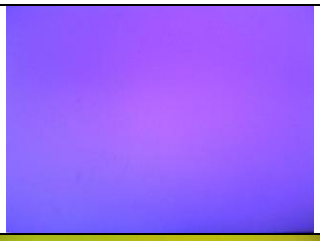
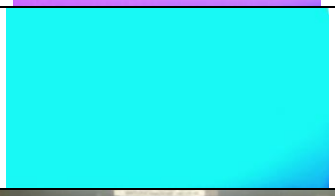
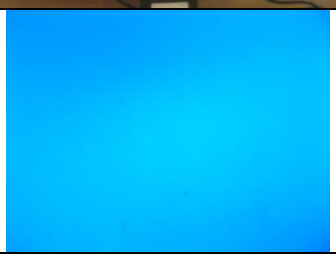
3.3 VGA interfacing Results

This work presents a VGA connector[2] that takes input from vgaController, and from twelve switches on the Digilent Nexys4 DDR Artix-7 FPGA[4] board (use switches as follows: r1_sw,r2_sw,r3_sw,r4_sw,g1_sw,g2_sw,g3_sw,g4_sw,b1_sw, b2_sw,b3_sw,b4_sw). Based on the value of these switches (i.e. Table 6), paint the entire 640x480 LCD screen to the color represented by the values on those switches. (Table 2).

Fig 11: Artix-7 FPGA Digilent Nexys4 DDR board

Table 6: LCD Output for different input combinations

Input Pattern – Input switches (r1r2r3r4_g1g2g3g4_b1b2b3b4)	LCD Output
Before Programming	
After Programming	
1111_1111_1111	
1111_0000_0000	
0000_1111_0000	

0000_0000_1111	
1111_1111_0000	
1111_0000_1111	
0000_1111_1111	
0000_0000_0000	
0000_0001_1111	

4. Conclusion

In this paper describes VGA controller and it is used to establish an interconnection between a LCD screen and Artix-7 FPGA kit through VGA port to display various colours on the LCD Monitor. Various individual modules of VGA controller has been designed using verilog HDL, verified functionally using ModelSim, synthesized by the XILINX VIVADO DESIGN SUITE[3] synthesis tool, and finally binary net list file has been created. For synthesis the system using 28nm ARTIX-7 fpga (XC7A100T-1CSG324C).The detailed synthesis results and power results for the system design is as shown in table 1. The fpga clock frequency is 100 MHz. In the future, scalable multipoint VGA controller[15] can be designed for efficient generation and display of high quality, multiple resolution of video streams.

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References

[1] Radi H.R., Caleb W.W.K., M.N.Shah Zainudin., M.Muzafar Ismail, "The Design and Implementation of VGA Controller on FPGA", International Journal of Electrical & Computer Sciences IJECS- IJENS, Vol. 12, Page(s) 56-60, 2012.

[2] Van-Huan Tran, Xuan-Tu Tran, "An Efficient Architecture Design for VGA Monitor Controller", IEEE International Conference on Consumer Electronics, Communications and Networks (CECNet), Page(s) 3921-3927, 2011.

[3] "Ultrafast Design Methodology Guide for the Vivado Design suite", UG949(v2015.1) June 1,2015 by www.xilinx.com

[4] "Nexys4 DDR FPGA Board Reference Manual"(rev.c), Revised September 11, 2014 by www.digilentinc.com

[5] "7 series FPGAs packaging and pinout product specification", UG475(v1.9), February 14,2013 by Xilinx.

[6] "Getting started with Artix-7 FPGAs", wp415(v1.0.1), March 27,2012 by Nick Mehta and Martin Gilpatric.

[7] CAST. "High Resolution Display Controller – Datasheet". Technical report, October 2010.

[8] "Think Silicon Ltd. Think LCD Display Controller – Product Specification." Technical report, 2010.

[9] Chacko B.T, Shelly S., "Real-Time Video Filtering and Overlay Character Generation on FPGA Recent Trends in Information", IEEE International Conference on Telecommunication and Computing (ITC), Page(s): 184 - 189 , March,2010.

[10] Richard Herveille. "VGA/LCD Controller v2.0." Technical Report, 2009.

[11] Guohui Wang, Yong Guan, and Yan Zhang. "Designing of VGA Character String Display Module Based on FPGA.", IEEE International Symposium on Intelligent Ubiquitous Computing and Education(IUCE), Page(s) 499–502, 2009.

[12] Javier Valcarce Garcia. "Monochrome Text-Mode VGA Video Display Adapter." Technical Report, 2009.

[13] Xilinx. "XPS Thin Film Transistor (TFT) Controller v1.00a." Technical Report, Product Specification, July 2008.

[14] Lung C.," Communication Control System Implemented in FPGA", IEEE International Symposium for Design and Technology in Electronic Packaging (SIITME), Page(s) 245-248, 2011.

[15] Thompson S., "VGA—Sign Choices for a New Video Subsystem", IBM Systems Journal Vol.27, Issue. 2, Page(s) 185-190, 1988.

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