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DELAY EFFICIENT BINARY ADDERS IN QCA

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Abstract

Quantum dot Cellular Automata(QCA) is an abstract model of Quantum computation, devised in analogy to conventional models of cellular automata. QCA have attracted a lot of attention as a result of its extremely small feature size and its ultra low power consumption, making it one candidate for replacing CMOS technology.

As size of the transistors decreases more, then we can accommodate more number of transistors in a single die, by this increase in chip computation capabilities. However , the size of the transistor cannot becomes smaller. One of the possible approach that represents solutions in overcoming this physical limit is Quantum-dot cellular automata(QCA).In this brief, we propose a 64bit adder that achieves the best delay trade off.

KeyWords: *Adders, Nano computing, Quantum-dot Cellular Automata(QCA).*

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1. INTRODUCTION

PQCA is a novel emerging technology in which logic states are not stored as voltage levels, but rather the position of individual electrons. Conceptually, QCA represents binary information by utilizing a bi-stable charge configuration rather than a current switch . A QCA cell can be viewed as a set of four "dots" that are positioned at the corners of a square .

A quantum dot is a site in a cell in which a charge can be localized . The cell contains two extra mobile electrons that can quantum mechanically tunnel between dots, but not cells. In the ground state and in the absence of external electrostatic perturbation, the electrons are forced to the corner positions to maximise their seperation due to the Coulomb repulsion. The two possible charge configurations are used to represent binary "0" and "1".

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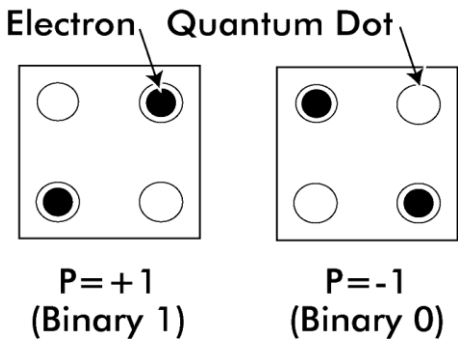

Fig. 1 QCA Cells

2. BACKGROUND

QCA is a nanostructure consists basic cell of a square four quantum dots structure charged with two free electrons able to tunnel through the dots within the cell. The two electrons will always reside in opposite corners due to the Coulombic repulsion. 1 and 0 are the two possible states that can be associated to the binary states determined by the locations of the electrons in the cell. Although adjacent cells interact through electrostatic forces and tend to align their polarizations, QCA cells do not have intrinsic data flow directionality.

The cells within a QCA design are partitioned into the so-called clock zones that are progressively associated to four clock signals, each phase shifted by 90 degrees to achieve controllable data directions. This clock scheme, named zone clocking scheme , makes the QCA designs intrinsically pipelined , as each clock zone behaves like a D-latch.

The basic logic gate for a quantum dot cell is MAJORITY GATE(MG). Majority gate and inverter(NOT) gate are considered as the two most fundamental building blocks of QCA. Fig. 2. shows a majority gate with three inputs and one output. In this structure, the Electrical field effect of each input on the output is identical and additive, with the result that whichever input state("binary 0" and "binary 1") is in the majority becomes the state of the output cell. For example, if input A exist in "binary 0" state and the inputs B and C exists in "binary 1" state since the combined Electrical field effect of inputs B and C together is greater than that of input A alone.

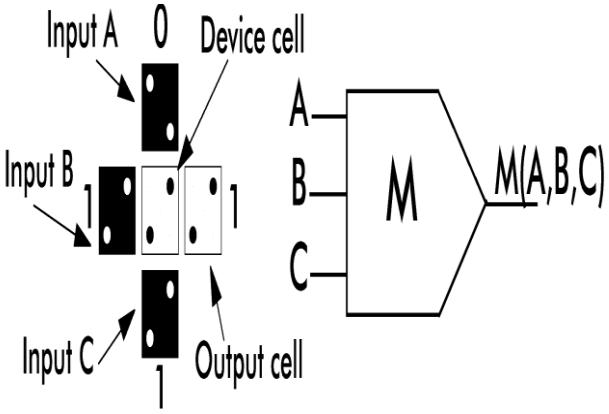

Fig 2 A QCA majority gate

QCA cells are used for both logic structures and interconnections that can be exploit coplanar cross or the bridge technique. The fundamental logic gates inherently available within the QCA technology are the inverter and the MG. Given three inputs a, b and c, the MG performs the logic function that provides all input cells are associated to the same clock clk (x) [x ranges from 0 to 3], whereas the remaining cells of MG are associated to the clock signal clk(x+1)

$$M(abc) = a \cdot b + b \cdot c + a \cdot c$$

The basic 2-bit module of QCA using majority gate are as shown in the Fig. 3

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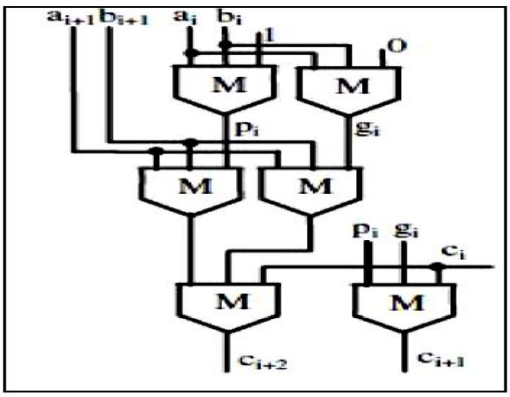

Fig. 3 Novel 2-bit basic module

The novel 2-bit module shows the computation of the carry ci+1 = M(pigici). The n-bit adder is then implemented by cascading n/2 2-bit modules. The carry-in of the adder is cin = 0, the signal p0 is not required and the 2-bit module used at the least significant bit position is simplified. The sum bits are finally computed. It must be noted that the time critical addition is performed when a carry is generated when a carry is generated at the least significant bit position (i.e.,g0 = 1)and then it is propagated through the subsequent bit positions to the most significant one.

In this case, the first 2-bit module computes c2, contributing to the worst case computational path with two cascaded MGs. The subsequent 2-bit modules contribute with only one MG each, thus introducing a total number of cascaded MGs equal to (n-2)/2. considering that further two MGs and one inverter are required to compute the sum bits, the worst case path of the novel adder consists of (n/2) + 3 MGs and one inverter.

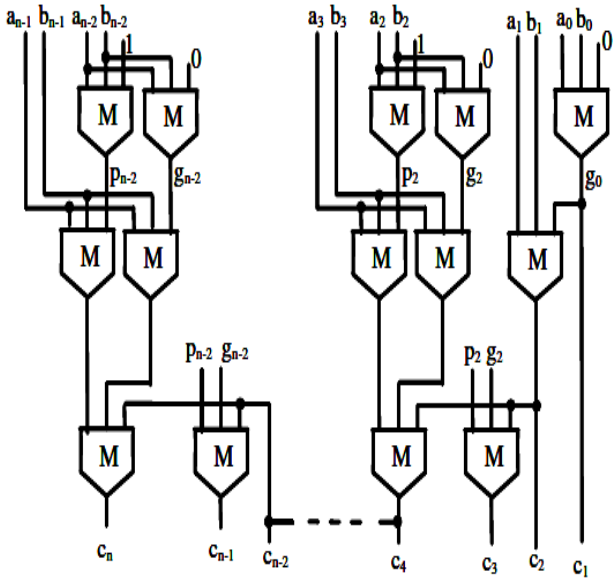

Fig. (a) Carry Block of n-bit adder

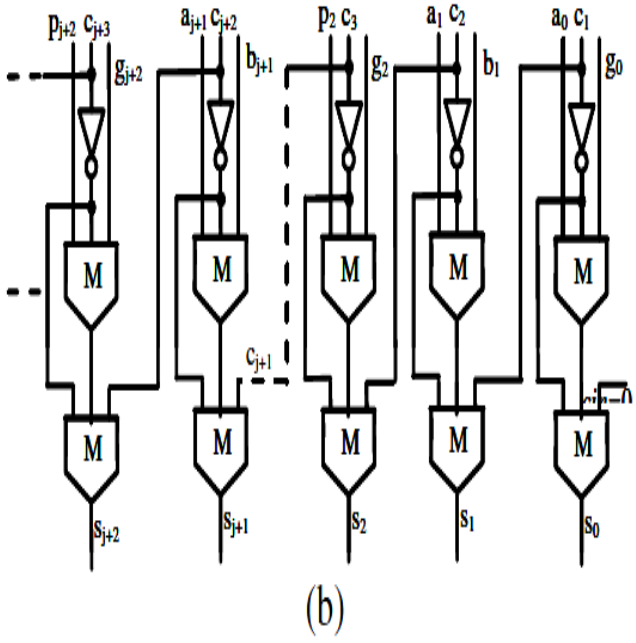

Fig. (b) Sum Block of n-bit adder

3. RESULT

The proposed addition architecture is implemented for several operands word lengths using QCA . The QCA cells are 18 nm wide and 18 nm high; the cells are placed on a grid with a cell center-to-center distance of 20 nm; there is at least one cell spacing between adjacent wires; the quantum dot diameter All paragraphs must be indented. All paragraphs must be justified, i.e. both left-justified and right-justified. is 5 nm. A maximum of 16 cascaded cells per clock zone are assumed.

Fig. 4 indicates the Simulation code for the 64-bit adder using VHDL synthesis and Fig.5 indicates the Simulation result of the 64-bit adder using Model sim software.

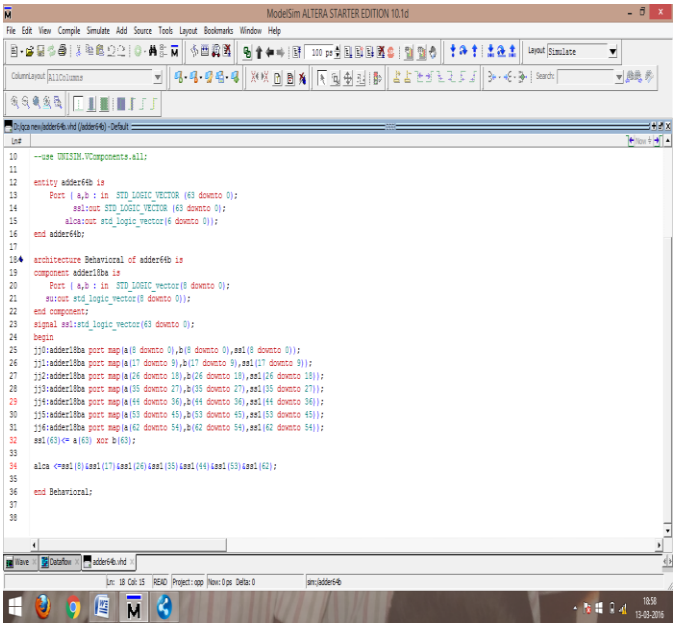

Fig. 4 Code for 64-bit adder

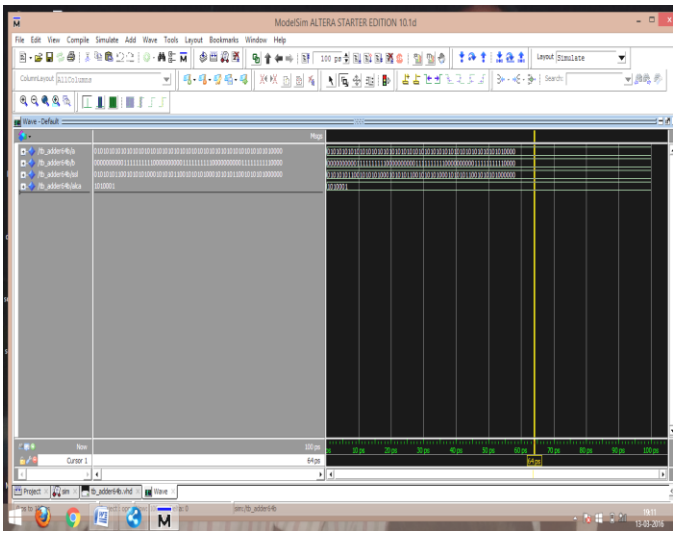

Fig. 5 Simulation result obtained for 64-bit adder

4. CONCLUSIONS

A new adder designed in QCA was presented. It achieves the speed performances higher than all the existing adders. A 64-bit binary adder designed as described in this brief exhibited a delay and occupied an active area. It achieved speed performances higher than all the existing QCA adders, with an area requirement comparable.

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BIOGRAPHIES

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