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A better transient response, better PSRR and low quiescent current capacitor-less low drop out regulator

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Abstract - *This paper presents a capacitor less LDO voltage regulator by varying the substrate voltage using IBM 90-nm technology which improves the performance of LDO voltage regulator by increasing the value of PSRR at high. Low drop out regulator (LDO) is a regulator which provide the difference between unregulated input and regulated output voltage while driving the load to its require range and also provide the require load current. LDO is an essential part of the power management system that provides constant voltage supply with improved transient response i.e. they should be capable of responding quickly to changes in load current. Increased demands of LDO make it important part of various fields like portable devices, biomedical devices, MCUs etc.*

Simulated results shows ΔV_{out} is less than 1 mV for 5 pF at 1uA load current with 54 uA quiescent current and 50 dB at 10KHz.

KeyWords:Capacitor-less,technology,PSRR,LDO,loadcurrent.

1. INTRODUCTION

The fundamental classes of voltage regulators are linear regulators and switching regulators. There are two basic types of linear regulator. One is the series regulator and the other is the shunt regulator. A simple representation of a series type of linear regulators. Linear regulators modulate the conductance of a series pass switch connected between an input dc supply V_{DD} and the regulated output V_{OUT} to ensure the output voltage is a predetermined ratio of its bias reference voltage. The term "series" refers to the pass element that is in series with the unregulated supply and the load. Since the current flow and its control are continuous in time, the circuit is linear and analog in nature, and because it can only supply power through a linearly controlled series switch, its output voltage cannot exceed its unregulated input supply (i.e.:$V_{OUT} < V_{DD}$). and stable DC voltage [2].

2. LITERATURE SURVEY

In the paper author's name AuLv Xiaopeng et al. presented a fully on-chip Low Drop-Out (LDO) voltage regulator with 150mA driving capability in 2014, which is implemented in 180 nm CMOS technology. This proposed LDO voltage regulator uses paralleled input differential pairs and current amplifiers to provide fast transient response, achieving 1.4μs settling time with transient variation less than 155mV, while consuming 90μA quiescent current [1].

In the paper author's name Herminio Martinez-Garcia et al. Have been investigate in 2013, A two stage cascoded operational transconductance amplifier is used to designed error amplifier by that achieve high DC gain and PSRR of 34.3 dB at 10 KHz [2].

In the paper author's name Leo C. J. et al. proposed an ultra low power capacitor less low drop out voltage regulator with High PSR of -95dB at 5MHz in 2013 is integrated with medical body area network (MBAN) transceiver having drop of 300mV and implemented on 0.13 μm CMOS IP6M process [3].

In the paper author's name Cheekala Lovaraju et. al. investigated a slew rate enhancement circuit is proposed in 2013 that improves the transient response and have high loop bandwidth with improvement in settling time by 61% [4].

In the paper author's name Fan Yang et al. design LDO that enhance the transient response using active feedback and damping factor control technique in 2014 which in turn use

to drive 50mA load with dropout of 200mV on 65nm CMOS process [5].

3. PROBLEM FORMULATION AND OBJECTIVES

The problem encountered in the performance of LDO is that the low power devices such as laptop, smart phones, medical devices, micro-controller units etc. consume large load current and during working as well as sleep mode, they have been leakaging large current which causes the low battery life.The objective of our paper is to increase the values of slew rate, PSR, load and line regulations and also decrease drop out voltage, quiescent current, settling time, area, and load current by using 90-nm technology.

4. THE PROPOSED LDO MODEL

In this figure 1, the substrate of the pass transistor is connected to the voltage source of 0.5V and gate of the pass transistor is connected to the output of the error amplifier. Therefore, the error amplifier will provide the high DC gain for accurate regulation. Error amplifier is just an operational amplifier which is made up of folded cascade type because this amplifier provides high slew rate and power supply rejection ratio. It also solves the problem of limited bandwidth of conventional LDO

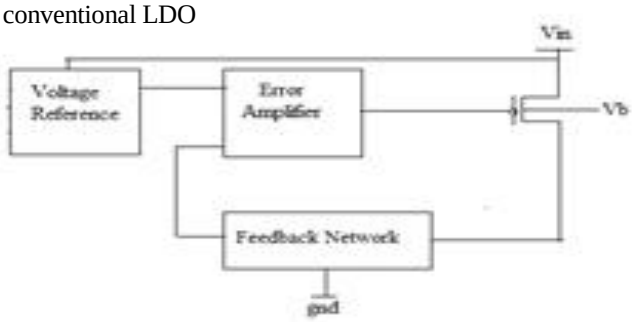

Fig -1: Diagram of proposed LDO

5. RESULTS

5.1 PSRR

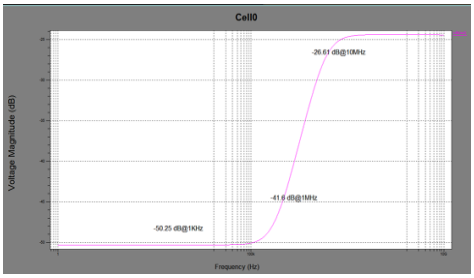

Fig -2: PSRR is shown for 10KHz,1MHz and 10MHz

Figure 2 indicates that at 10KHz, PSRR is 50dB which is better result as compared to [2] & [5] and it's has application in area's where noise is of major concern.

5.2 Transient Response

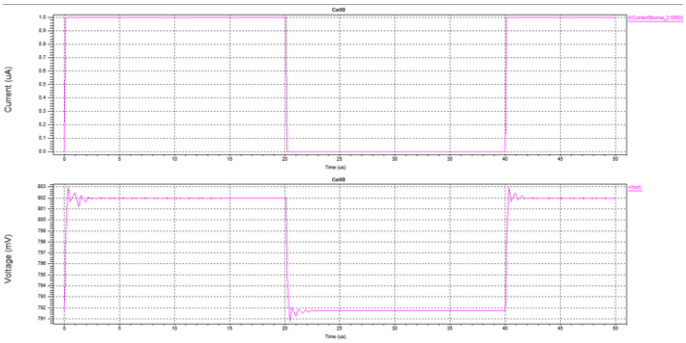

Fig -3: transient response for 1uA load current.

Figure 3 show the simulation results illustrate that the output voltage variation is 995uV, 935uV respectively; with settling time of 2.3µs, 2.7µs for 5pF at 1uA load current which is again better result as compare to [4] & [6] .

5.3 Quiescent Current

Quiescent current is the difference between input and ouput current and this has to be very low. So this LDO has quiescent current of 54uA which is the better in comparison to [1].

6. CONCLUSION

A low drop out voltage regulator has been designed on 90 nm and simulated in Tanner EDA software. To improve the performance of LDO voltage regulator, threshold voltage of pass transistor has been modulated by varying substrate voltage of 700 mV, which regulates the output voltage at 0.9 V from 1 V supply with minimum drop-out voltage of 100 mV and delivering maximum output current of 1 uA. The use of this technique allows us to achieve high PSRR, which has found out to be 50 dB at 10 KHz . Within the scope of power management system low quiescent current consumption is required which is 54 µA and ΔV_{out} is less than 1 mV for 5 pF at 1uA load current.

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