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PERFORMANCE ANALYSIS OF JUNCTIONLESS SONOS MEMORY

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Abstract - *This paper presents the performance analysis of a junctionless (JL) flash memory built on bulk substrate wafer and its comparison with the silicon-on-insulator (SOI) counterpart. The extensive two dimensional simulations have been performed on both type of memory device and their characteristics are compared and discussed in detail. The effects on device characteristics, due to physical and electrical parameter variations in the memory device, have been elaborated. Bulk doping parameter can be used as one of the tuning parameter to achieve the required memory performance.*

Key Words **: Silicon-On-Insulator (SOI), Fowler-Nordhiem (FN), Shockley-Read-Hall (SRH), Junctionless (JL), Silicon-Oxide-Nitride-Oxide-Silicon (SONOS), Technology Computer Aided Design (TCAD), Silicon Nanowire (Si-NW), Equivalent Oxide Thickness (EOT).**

1. INTRODUCTION

The non-volatile flash memory device can be fabricated on either p-type silicon substrate (termed as 'bulk') or on the silicon-on-insulator substrate. The performance of the device is different for different kind of substrate and the choice of device substrate depends on the advantage of one over the other. The implementation cost of device on bulk-silicon wafer is economical than the SOI wafer. So, it is effective to fabricate the device on bulk wafer to reduce the device substrate cost and to maintain the minimum memory fabrication cost. Moreover, the bulk wafer compatibility with the industry fabrication process flow is better and the scalability of device is easier [1]. But the SOI wafer provides easier realization of device having minimum parasitic junction capacitance. It helps in easy isolation to allow higher integration for better chip density.

The investigation on the device performance built over any one of the substrate is carried out using 2-D device simulation to evaluate the program and erase characteristics of both devices while maintaining similar device dimensions and parameter values during simulation. Moreover, the bulk substrate type device metrics such as program/erase (P/E) efficiency, at different substrate (N_{bulk}) and nanowire doping (NW_{dop}) have been analyzed and it can be used as one of the memory window optimization parameter.

First, we carried out 2-D numerical simulation using commercial Silvaco TCAD tool to investigate the accurate simulation results of both bulk and SOI based JL SONOS at nanoscale device dimensions. The simulation is carried out using Fowler-Nordhiem (FN) tunneling, drift-diffusion transport model, Shockley-Read-Hall (SRH) trapping/detrapping model, Poole-Frenkel and trap dynamic models. The tunneling and blocking oxide layers in the gate stack are considered as a pure tunnel barrier (without traps) for simplicity. Uniformly distributed traps are located throughout the silicon nitride region for the charge storage. The parameter values for different models incorporated in simulation are listed in Table 1.

Table 1: List of parameters for simulation

Parameters	Value
SiO_2 relative dielectric constant	3.9
Si_3N_4 relative dielectric constant	7.5
Si relative dielectric constant	11.8
SiO_2 electron affinity	0.9eV
Si_3N_4 electron affinity	2.6eV
Si electron affinity	4.05eV
SiO_2 band gap	9.0eV
Si_3N_4 band gap	5.3eV
Si band gap	1.12eV
SiO_2 effective mass	$0.4m_o$
Si_3N_4 effective mass	$0.4m_o$
Gate work function	5.25eV
Si_3N_4 electron/hole trap energy	1.5eV
Si_3N_4 electron/hole trap cross section	1.e-10 cm^{-2}
Si_3N_4 electron trap density	1.e+20 cm^{-3}

Figure 1(a) and 1(b) presents the simulated device structure of n-channel JL SONOS with bulk and SOI substrate, respectively. In figure 1(a), the n-type silicon nanowire (Si-NW) of thickness (T_b) 10 nm is made over the p-type silicon substrate (bulk) having doping concentration (N_{bulk}) equal to 1×10^{18} cm^{-3} unless otherwise specified. At the top of the Si-NW, the gate stack consists of tunnel oxide (SiO_2), silicon nitride (Si_3N_4) and top control oxide (SiO_2) having widths 2 nm, 5 nm and 5 nm, respectively. Figure 4.1(b) shows the SOI JL SONOS structure with the same device dimensions as

depicted in figure 1(a). It has a buried oxide (BOX) isolation layer between the bulk and the Si-NW of thickness (T_{si}) 10 nm. Both the devices have uniform n-type doping i.e. source, drain and channel are doped with same concentration of 1 X 10^{19} cm^{-3} and have gate stack with the equivalent oxide thickness (EOT) of 9.6nm, which is calculated by equation as follows:

$$EOT = T_{box} + T_n\left(\frac{\epsilon_{ox}}{\epsilon_n}\right) + T_{tox}$$

where,
T_{box}, T_n, T_{tox} = bottom oxide, nitride and top oxide thickness, respectively and
ϵ_{ox}, ϵ_n = dielectric constants of oxide and nitride, respectively.

For highly doped Si-NW channel, it often requires the gate electrode with a high work function value so as to obtain the desirable threshold voltage. Hence, the p-type polysilicon material is used as the gate electrode in both the devices. The source and drain contacts are also taken as a polysilicon material.

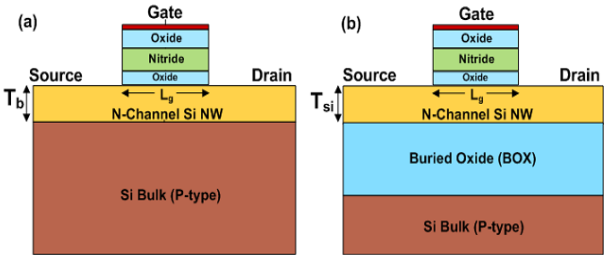

Figure 1: Schematic representation of the (a) JL bulk SONOS and the (b) JL SOI SONOS, respectively. T_b=T_{si}= 10 nm, L_g= 100 nm, $N_{si\text{-}NW}$ = 1 X 10^{19} cm^{-3} (uniform doping), N_{bulk} = 1 X 10^{18} cm^{-3} (p-type), O/N/O = 2/5/5 nm.

The program and erase mechanisms were performed using FN tunneling to obtain the memory performance characteristics. In the programming process, the source, drain and substrate terminals are grounded and higher positive stress voltage (V_{gp}) is applied to the gate which induces large electric field across tunnel oxide and assists the carriers to tunnel from the channel to the nitride layer. To erase the device, first it is programmed for 100 ms to obtain a desired value of threshold voltage shift relative to un-programmed (fresh) device. Then, a negative bias is applied to the gate with the source/drain (S/D) and substrate terminal remains grounded. The threshold voltage variation depends on the applied gate bias and the program time which in turn causes the corresponding changes in the electric field across the tunneling and blocking oxide layers. It reveals that the JL device exhibits efficient program characteristics due to higher electron concentration in the channel region, but it suffers from slower erase speed due to reduced hole concentration in the channel region [2], which makes it suitable for the improved memory performance as compared to conventional SONOS device.

2. SIMULATION & RESULT

This section would deal with the program and erase characteristics of both the device built on bulk and SOI silicon wafer. The variation of the threshold voltage for different time is observed and performance comparison is done with its counterpart device.

4.3.1 Transfer Characteristics

The transfer characteristics (I_d-V_{gs}) of both SONOS device at fresh and programmed state with V_{gp}= 14 V are shown in figure 2 and 3 with the nanowire width of 10 nm and doping value of 1 X 10^{19} cm^{-3}.

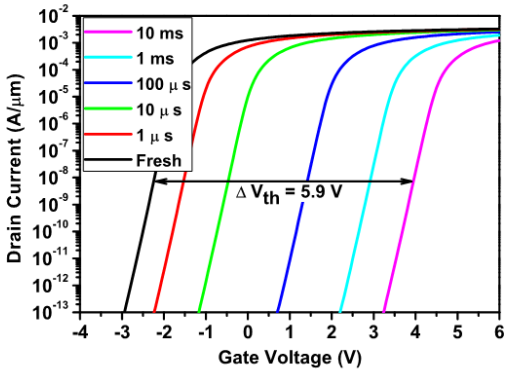

Figure 2: I_d-V_g characteristics of planar JL bulk SONOS memory (L_g= 100 nm and T_b= 10 nm) at the gate bias voltage V_{gp}=14 V, O/N/O=2/5/5 nm.

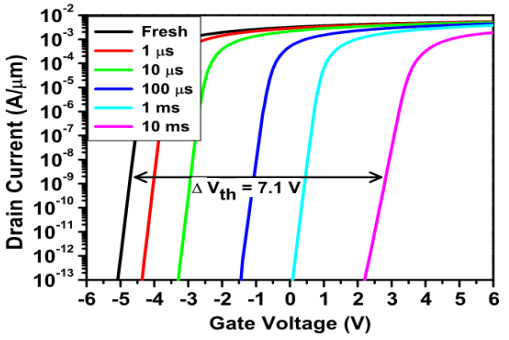

Figure 3: I_d--V_g characteristics of planar JL SOI SONOS memory (L_g= 100 nm and T_b= 10 nm) at the gate bias voltage V_{gp}=14 V, O/N/O=2/5/5 nm

This would help in calculating the total threshold voltage (V_{th}) shift during specified program time at a particular gate voltage. The difference between the V_{th} value of the programmed and the fresh device is referred as memory window of the device and it should be large enough to distinguish two different logic level. Higher memory window value also makes the possibility of multi bit information storage in a memory cell. It can be seen that all the transfer

curves shift in parallel during programming for the charging time of 10 ms to obtain the memory window of 7.1 V and 5.9 V for the SOI and bulk devices, respectively. The SOI device offer large memory window and can be utilized for multi-level storage as compared to bulk.

4.3.2 Program Operation

In this section, the typical performance metrics like program characterization is discussed for the JL memory device built on SOI and bulk substrate. The memory devices with the channel length (L_g) of 100 nm, Oxide-Nitride-Oxide (O/N/O) stack thickness of 2/5/5 nm and T_{si}=T_b= 10 nm are employed in the analysis. Figure 4 and 5 show the variation of threshold voltage shift with the program time at gate bias voltages (V_{gp}) ranging from +10V to +14V for SOI and bulk substrate, respectively.

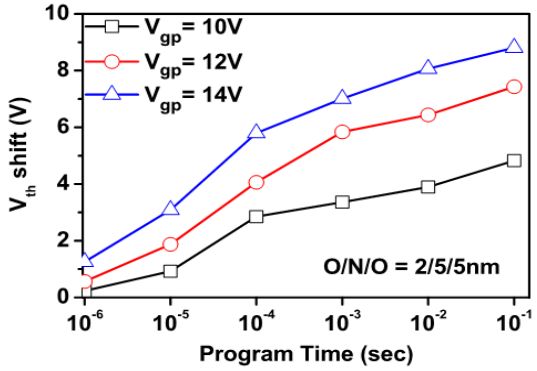

Figure 4: Programming characteristics of planar JL SOI SONOS (L_g= 100 nm and T_{si}=10 nm) at different gate bias voltage (V_{gp}), O/N/O=2/5/5 nm.

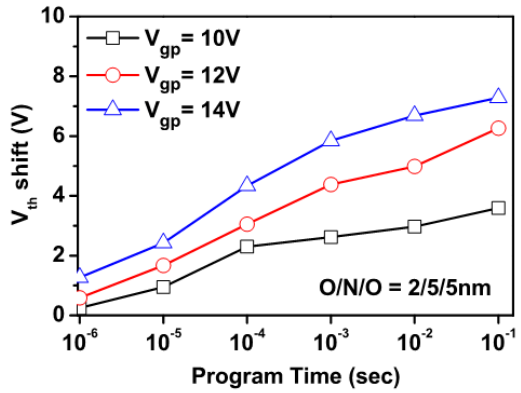

Figure 5: Programming characteristics of planar JL bulk SONOS memory (L_g= 100 nm and T_b= 10 nm) at different gate bias voltage (V_{gp}), O/N/O=2/5/5 nm.

It can be analyzed that the SOI substrate device exhibits a greater V_{th} shift of 8.8 V in 100 ms at a gate voltage of +14 V as compared to 7.2 V for same program time and gate voltage for the bulk counterpart.

It has been noticed that during programming of each gate bias, the bulk substrate device depicts lower threshold voltage shift as compared to the SOI counterpart. Such observation might be related to the effective "active channel layer" thickness that reduces due to the induced depletion region at channel/substrate junction [3]. As a result, the net electron concentration will be reduced and the programming performance is affected. The variation of electron concentration along the channel area from top to bottom (bottom of ONO stack to top of the substrate) is shown in figure 6 for both type of substrate. Figure 6 shows constant electron concentration in channel area for SOI but in case bulk substrate case, the electron concentration goes on decreasing with the increase in distance.

This variation is due to the diffusion across the bulk (p-type) substrate and highly doped channel area. On the other hand, in SOI there is no junction formation between channel and substrate which follows that the carrier concentration would remain constant in channel area. This would improve the threshold voltage shift that is attributed to the higher electron carrier concentration in the conduction band of NW-channel, which results in increasing the tunneling probability of electrons into the trapping layer (nitride) [4]. Hence, faster programming with enhanced program memory window is obtained for SOI substrate. Moreover, the minimum threshold voltage shift that we have achieved for SOI substrate is 20% more when compared to that of bulk substrate device.

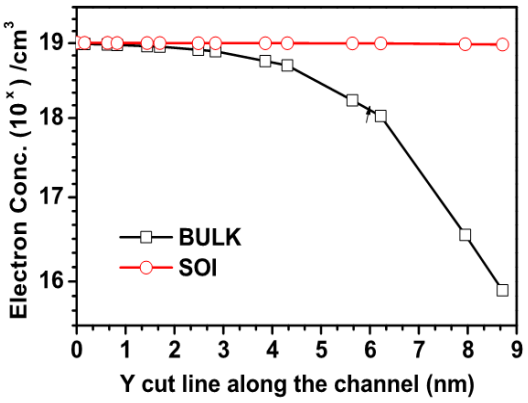

Figure 6: Electron concentration in the vertical direction along the channel area from gate to substrate for SOI and bulk substrate respectively.

4.3.3 Erase operation

Figure 7 and 8 represent the erase properties of SOI and bulk JL SONOS, respectively, which shows the variation of threshold voltage shift with the erasing transient time at different gate stress voltages (V_{ge}). In order to study the erase behavior, the memory cell is first programmed with the gate voltage (V_{gp}) of 14 V for 100 ms duration to reach at the particular V_{th} shift level i.e. 2.0 V for SOI and 4.5 V for bulk

and then the erasing characteristics are obtained by applying negative gate voltages (V_{ge}) ranging from -10 V to -12 V for time span of 0.1 μs to 100 ms. In every JL SONOS devices, the electron detrapping and hole injection mechanism are the major constituents of the erasing current, which is mainly affected due to the band alignment positions.

It clearly noticed that, up to 1.0 ms erase time, the bulk type device exhibits faster erasing speed than the SOI counterparts. Afterwards, it is evident that the difference in erasing speed between the two devices is not as remarkable. It is due to the change in net concentration of holes on Si-NW channel when the p-type bulk is introduced. The diffusion due to concentration gradient between bulk and channel improves net hole concentration in Si-NW channel and hence erase phenomena is quite fast in bulk. Moreover, the erasing characteristics of SOI type device shows the weak dependencies on the applied erase gate voltage.

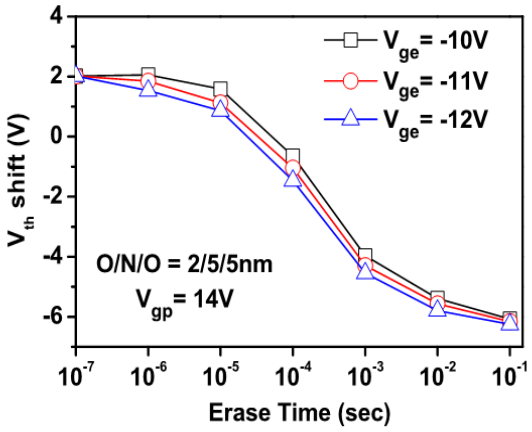

Figure 7: Erase properties of planar JL SOI SONOS memory cell. (L_g= 100 nm and T_{si}= 10 nm) at different gate erase voltage (V_{ge}).

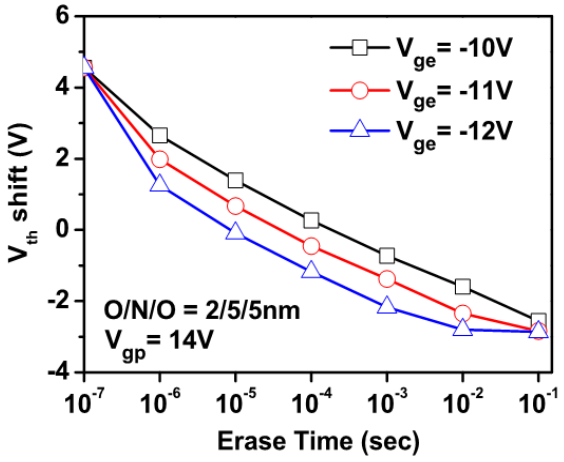

Figure 8: Erase properties of planar JL bulk SONOS memory cell (L_g= 100 nm and T_b= 10 nm) at different gate erase voltage (V_{ge}).

4.3.4 Retention Characteristics

The one most prominent feature of the memory device is the retention characteristics, which indicates about the lifetime of the stored information. Higher the retention time higher would be its charge retaining capacity. With the span of time, when the memory is kept in idle state after its programming, the stored charges get reduced as the time gets elapsed. It is due to the leakages of stored charge through the defected oxide layers above and below the charge trapping layer. Figure 9 shows the retention characteristics of both the devices under same programming and retention testing conditions. The device is first charged with the gate voltage V_{gp}= 14 V applied for 100 ms and then all the terminals remained open to analyze the discharging property. Both the device shows almost same discharging behavior, which indicates that the substrate alteration could not affect the retention time of the memory device. The retention mainly depends on the tunnel oxide thickness and the band offset values of the Si and Oxide materials. As a result, the retention characteristics does not have any dependency on different substrate wafer type.

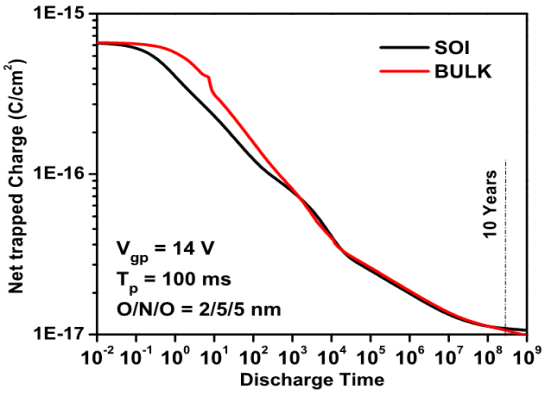

Figure 9: Retention characteristics of both type of planar JL SONOS memory device (L_g= 100 nm and T_b= 10 nm), when first program at V_{gp}= 14 V for 100 ms and then open S/D and substrate terminals.

After the comparative study of program, erase and retention characteristics of both type of SONOS memory, the further section would discuss about the effect of Bulk substrate and nanowire channel doping on the program properties of the memory device.

4.3.5 Bulk Doping Sensitivity

In order to investigate the effect of the substrate doping (N_{bulk}) on the V_{th} variation, the V_{th} shift and program time at a stress voltage V_{gp} = 14 V was obtained as shown in figure 10, by varying the doping concentration of the substrate ranging from 6 X 10^{16} cm^{-3} to 9 X 10^{17} cm^{-3} . It can be clearly marked that the higher bulk doping shows lower threshold voltage shift. At the doping of 9 X 10^{17} cm^{-3}, the V_{th} shift is about 7.2 V for 100 ms charging time and the doping of 6 X 10^{16} cm^{-3} gives 8.0 V V_{th} shift, which is approximately 11% higher. The possible reason for this V_{th} deviation in the bulk device could be ascribed to the diffusion of carriers towards the channel area from the substrate end, which tends to reduce the net

electron density in the channel area. As a result, the total threshold voltage shift decreases, and hence memory window gets reduced. In this way, the P/E window can be optimized according to the doping concentration.

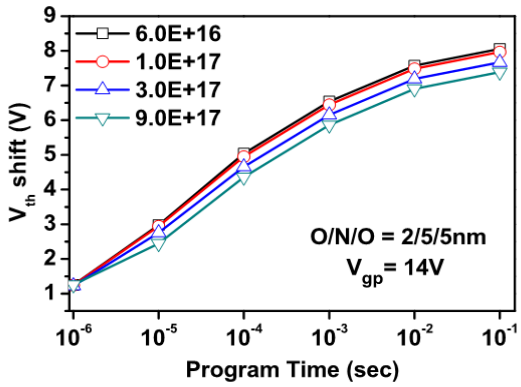

Figure 10: Program characteristics of planar JL bulk SONOS memory (L_g= 100 nm and T_b= 10 nm) at different substrate doping concentration (6 X 10^{16} cm^{-3} to 9 X 10^{17} cm^{-3}). The positive gate voltage (V_{gp} = 14 V) is applied while maintaining the S/D at the ground potential for FN tunneling.

4.3.6 Nanowire doping effects on Threshold voltage shift

Figure 11 illustrates the Program characteristics of the SOI memory cell to analyze the impact of Si-NW doping concentration on the V_{th} shift. The device is programmed at two different gate stress voltages of +12 V and +14 V with the channel doping of 5 X 10^{18} cm^{-3} and 1 X 10^{19} cm^{-3} at a fixed NW width of 10 nm. It can be observed that the higher NW doping concentration exhibits quiet larger threshold voltage shift at both the gate stress voltages. Higher doping provides abundance of carriers in the channel region to enhance the electron tunneling probability and hence leads to better programming efficiency.

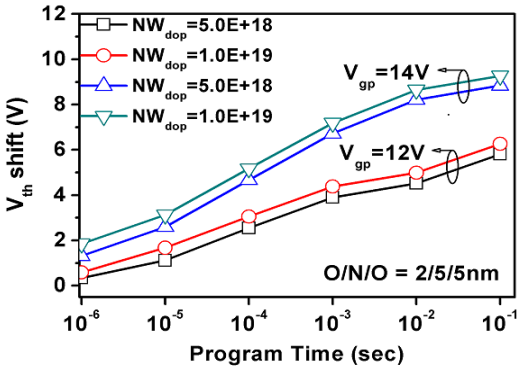

Figure 11: Program characteristics of planar JL SOI SONOS memory (L_g= 100 nm and T_b= 10 nm) at two different nanowire doping concentration (5 X 10^{18} cm^{-3} to 1 X 10^{19} cm^{-3}). The positive gate voltage (V_{gp} = 12 V and V_{gp} = 14 V) is applied while maintaining the S/D at the ground potential for FN tunneling.

At the end, chapter concludes with the investigation of P/E characteristics of JL NW SONOS device with SOI and bulk substrate. The results of 2-D device simulation have compared the SOI device with the bulk counterpart. The SOI devices exhibits faster programming behavior and can be operated with a much reduced program voltage. On the other hand the erase performance of bulk substrate over a specified erase time is quiet faster in bulk. Additionally, in bulk type SONOS, the effective channel thickness is reduced due to the formation of channel/substrate junction. One additional parameter i.e. substrate doping concentration (N_{bulk}) can be adjusted to get optimized memory device performance in case of bulk. Moreover, the affect of NW doping on program characteristics have been discussed for the bulk type device.

3. CONCLUSIONS

The JL memory device has been built over silicon bulk (p-type) and its comparison with SOI type SONOS device has been discussed in detail and have made the following conclusions: (a) SOI device shows better program performance with higher threshold voltage shift, (b) The erasing is efficiently done with the bulk type device, i.e. the device can be fully erased due to more hole concentration, and (c) The retention is same for both type because the retention mainly depends on the ONO stack width and it is considered same for both devices. These parameters would be adjusted so as to make the device performance efficient.

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