Design & Analysis of ANFIS Controller for Three Phase UPS System under Unbalanced Loads & Distorted grid voltages

Y. Harish Babu[1], M. Rama Sekhara Reddy[2]

[1]*Student, Dept. of Electrical and Electronics Engineering, JNTU College of Engineering, Ananthapur, AP, India.*

[2]*Assistant Professor, Dept. of Electrical and Electronics Engineering, JNTU College of Engineering, Ananthapur, AP, India.*

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Abstract: This paper proposes a basic ideal voltage control technique for three-stage uninterruptible-control supply frameworks. The proposed voltage controller is made out of a criticism control term and a repaying control term. The previous term is intended to make the framework blunders unite to zero, though the last term is connected to make up for the framework instabilities. In addition, the ideal load current spectator is used to streamline framework cost and dependability. Completely, the shut circle soundness of an onlooker predicated ideal voltage control law is numerically demonstrated by displaying that the entire conditions of the increased eyewitness predicated control framework mistakes exponentially unite to zero. Not at all like forerunner calculations, the proposed strategy can make a tradeoff between control input greatness and following blunder by just winnowing fitting execution records. The viability of the proposed controller is approved through reproductions. Determinately, the similar results for the proposed conspire and the traditional input linearization control plan are displayed to show that the proposed calculation accomplishes a superb execution, for example, quick transient replication, minute enduring state mistake, and low aggregate consonant contortion under load step change, unequal load, and nonlinear load with the parameter varieties.

Key Words: : *Adaptive Neuro Fuzzy Interface System (ANFIS),Optimal stack current eyewitness, ideal voltage control, three-stage inverter, add up to symphonious mutilation (THD), uninterruptible power supply (UPS).*

I INTRODUCTION

With the advancement of data innovation, uninterruptible power supply (UPS) frameworks have turned out to be extremely prevalent together with the instruments of PCs, therapeutic/life-emotionally supportive networks, media transmission and modern controls. At the point when the utility lattice control has a dropout, the PC control supply can debase and the PC may crash. On the off chance that the info A source has lists and surges, the PC may incite blunder message. To keep up a top notch energy to the heaps, for example, PCs and correspondence gear, UPS is ineluctable. An elite UPS framework ought to have an unsullied yield voltage with low aggregate symphonious contortion (THD) for both straight and nonlinear burdens, high proficiency, awesome dependability and quick transient replication for sudden power lattice disappointment and load changes. Regardless of varieties in the information source or load condition, keeping up a steady voltage and consistent recurrence supply for basic burdens, is the real capacity of an UPS (Senthil Kumar et al 2010). UPS supplies, the required uninterruptible AC

to straight and nonlinear burdens. In synopsis, a perfect UPS ought to have the accompanying elements. Directed sinusoidal yield voltage with low THD and autonomous from the transmutations in the information voltage or in the heap, on-line operation that means zero changing time from commonplace mode to move down mode and the other way around, low THD sinusoidal info current and solidarity control calculate, high unwavering quality, high efficiency, lowelectromagnetic interference (EMI) and acoustic noise, electric segregation, low upkeep, and minimal effort, weight, and size.

Diode rectifier, Pulse Width Modulation (PWM) inverter, input/yield channel, DC-connect capacitor, battery charger and battery, battery on/off switch, and load transformer are the significant segments of this framework (Praveen K.Jain et al 1998). For the DC–AC transformation, a full-connect PWM inverter is utilized. A channel is used to get the sinusoidal waveform from the PWM altered heartbeat waveform (Sunil Kumar Gupta et al 2010). A change is used to shield the battery from lifted current levels that surpass the assignments of the battery maker (Nimrod Vazquez et al 2002).

The topology jars work in two distinct modes, in particular, ordinary/charging and reinforcement modes (Praveen K.Jain et al 1998). In the everyday/charging mode, the battery on/off switch is opened. Thus, the air conditioner principle supplies the heap control all through the PWM inverter and charges the battery at steady present as well(Rajarajeswari et al 2008).A rectifier is used for changing over the air conditioner voltage into dc voltage, for charging Batteries (SenanM.Bashi et al 2009). In the reinforcement mode, the air conditioner primary is not accessible and the battery on/off switch is shut. Along these lines, the battery supplies the heap intensity.

Thusly, this paper proposes an onlooker predicated ideal voltage control conspire for three-stage UPS frameworks. This proposed voltage controller epitomizes two principle parts: a criticism control term and a repaying control term. The previous term is intended to make the framework blunders merge to zero, and the last term is connected to assess the framework instabilities. The Lyapunov hypothesis is used to examine the dependability of the framework. Uncommonly, this paper demonstrates the shut circle strength of an onlooker predicated ideal voltage control law by showing that the framework mistakes exponentially merge to zero. In addition, the proposed control law can be deliberately planned mulling over a tradeoff between control input extents and following blunder not at all like predecessor calculations [23]. The adequacy of the proposed control technique is confirmed by means of recreations on MATLAB/Simulink.

In this paper, an ordinary PI technique in [17] is winnowed to show the similar results since it has a decent execution under a nonlinear-stack condition, and its circuit model of a three stage inverter in [17] is likened to our framework display. Indisputably, the outcomes pellucidly demonstrate that the proposed ANFISscheme has a decent voltage direction capacity, for example, quick transient deportment, small unfaltering state mistake, and low THD under sundry load conditions, for example, stack step change, lopsided load, and nonlinear load in the subsistence of the parameter varieties.

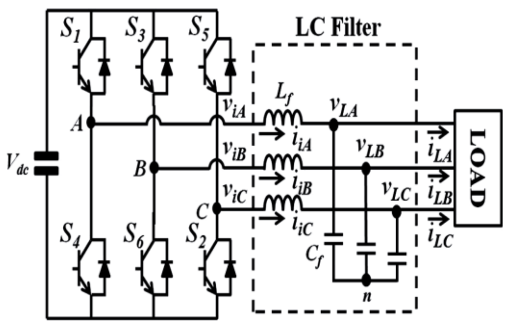


Fig. 1.Three-phase inverter with an *LC* filter for a UPS system.

II METHODOLOGY OF THE PROPOSED SYSTEM

The three-stage UPS framework with a LC channel is appeared in Fig. 1, which is made out of a dc-connect voltage (Vdc), a threephasepulsewidth balance (PWM) inverter (S1 ∼ S6), a yield LC channel (Lf, Cf), and a three-stage stack (e.g., straight or nonlinear load). In light of Fig. 1, the dynamic model of a three-stage inverter can be determined in a d − q synchronous reference outline as takes after [24]:

$$\begin{cases} \dot{i}_{id}=\omega i_{iq}+k_2 v_{id}-k_2 v_{Ld} \\ \dot{i}_{iq}=-\omega i_{id}+k_2 v_{iq}-k_2 v_{Lq} \end{cases}, \quad \begin{matrix} \dot{v}_{Ld}=\omega v_{Lq}+k_1 i_{id}-k_1 i_{Ld} \\ \dot{v}_{Lq}=-\omega v_{Ld}+k_1 i_{iq}-k_1 i_{Lq} \end{matrix} \quad (1)$$

where k1 = 1/Cf , and k2 = 1/Lf . In framework demonstrate (1), vLd, vLq, iid, and iiq are the state factors, and vid and viq are the control inputs. In this plan, the suspicion is made to develop the ideal voltage controller and ideal load current onlooker as takes after:

A. Design ofOptimal Voltage Controller

Here, a simple optimal voltage controller is proposed for system (1). First, let us define the *d* − *q*-axis inverter current references (*i*∗*id*, *i*∗*iq*) as

$$i_{id}^* = i_{Ld} - \frac{1}{k_1}\omega v_{Lq}^*, \quad i_{iq}^* = i_{Lq} + \frac{1}{k_1}\omega v_{Ld}^*. \quad (2)$$

Then, the error values of the load voltages and inverter currents are set as

$$v_{de} = v_{Ld} - v_{Ld}^*, \quad v_{qe} = v_{Lq} - v_{Lq}^*$$

$$i_{de} = i_{id} - i_{id}^*, \quad i_{qe} = i_{iq} - i_{id}^*. \quad (3)$$

Therefore, system model (1) can be transformed into the following error dynamics:

where $x = [v_{de}\ v_{qe}\ i_{de}\ i_{qe}]^T$, $u = [v_{id}\ v_{iq}]^T$, $u_d = [d_d\ d_q]^T$,

$$A = \begin{bmatrix} 0 & \omega & k_1 & 0 \\ -\omega & 0 & 0 & k_1 \\ -k_2 & 0 & 0 & 0 \\ 0 & -k_2 & 0 & 0 \end{bmatrix}, \quad B = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ k_2 & 0 \\ 0 & k_2 \end{bmatrix}$$

$$d_q = -v_{Ld}^* + (1/k_2)\omega i_{Lq}, \quad \text{and} \quad d_q = -v_{Lq}^* + (1/k_2)\omega i_{Ld}.$$

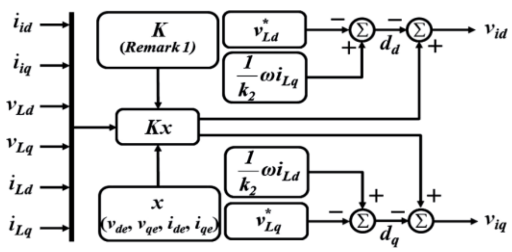


Fig.2 Block diagram of the proposed optimal voltage control scheme.

III OPTIMAL LOAD CURRENT OBSERVER DESIGN AND STABILITY ANALYSIS

As found in (2) and (4), the inverter current references (i∗ d and i∗ q) and nourish forward control term (ud) require stack current data as information sources. To abstain from utilizing current sensors, a direct ideal load current eyewitness is presented in this calculation. From (1) and the supposition, the accompanying element model is acquired to appraise the heap current:

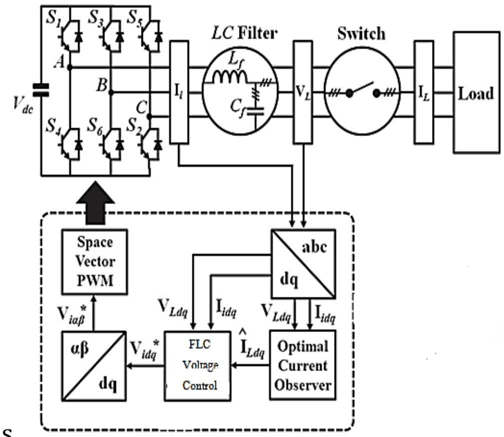
$$\begin{cases} \dot{x}_o = A_o x_o + B_o u_o \\ y = C_o x_o \end{cases}$$

where $x_o = [i_{Ld}\ i_{Lq}\ v_{Ld}\ v_{Lq}]^T$, $u_o = [k_1 i_{id}\ k_1 i_{iq}]^T$,

$$A_o = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -k_1 & 0 & 0 & \omega \\ 0 & -k_1 & -\omega & 0 \end{bmatrix},\ B_o = C_o^T = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 1 & 0 \\ 0 & 1 \end{bmatrix}.$$

$$\dot{\hat{x}}_o = A_o \hat{x}_o + B_o u_o - L(y - C_o \hat{x}_o)$$

Then, the load current observer is expressed



as

Fig.3 Block diagram of the proposed observer-based optimal voltage control system.

IV. DESIGN OF ADAPTIVE NEURO-FUZZY CONTROLLER

Adaptive neuro fuzzy inference system (ANFIS) incorporates the best elements of fluffy frameworks and neural systems, and it can possibly catch the advantages of both in a solitary edge work. ANFIS is a sort of simulated neural system that is predicated on Takagi-sugeno fluffy deduction framework, which is having one info a done yield. Using a given information set, the tool compartment capacity of ANFIS develops a fluffy deduction framework (FIS) where as the participation work parameters are tuned (balanced) using a back engendering calculation. With a specific end goal to have an origination of advanced ANFIS engineering for proposed control, an underlying information is induced from everyday PI controller and the information is protected in workspace of MATLAB. At that point the ANFIS order window is opened by inditinganfis editorial manager in the primary MATLAB window. At that point the information prior safeguarded in workspace is stacked in the ANFIS charge window to create an advanced ANFIS engineering as appeared in Fig.3.

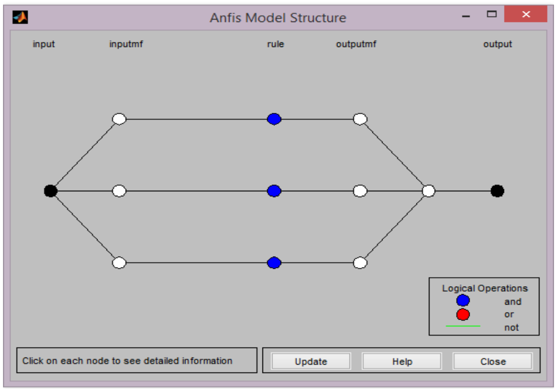


Figure.4Optimized ANFIS architecture suggested by MATLAB/anfiseditor.

In Fig.4 shows schematic of the proposed ANFIS based control architecture. The node functions of each layer in the ANFIS architecture are described as follows:

The mistake between reference dc-interface voltage and credible dc-connect voltage (ξ=Vdc*-Vdc) is given to the neuro-fluffy controller and a similar blunder is used to tune the precondition and ensuing parameters [10]. The control of dc-connection voltage gives the dynamic power current segment (id *'), which is further adjusted to assess dynamic current part infused from RES (iRen).The hub elements of every layer in ANFIS design are as portrayed beneath:

Layer 1: This layer is also kenned as fuzzification layer where every hub is spoken to by square. Here, three enrollment capacities are doled out to every information.

The trapezoidal and triangular enrollment capacities are utilized to reduce the computation burden as shown in Fig.5. And the corresponding node equations are as given below:

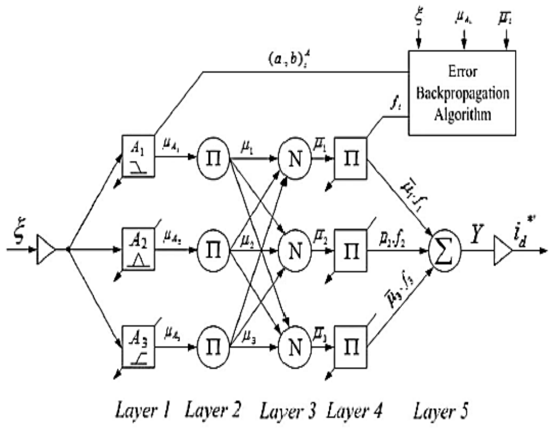


Fig.5 Schematic of the proposed ANFIS-based control architecture.

$$\mu_{A1}(\varepsilon) = \begin{cases} 1 & \varepsilon \le b_1 \\ \frac{\varepsilon - a_1}{b_1 - a_1} & b_1 < \varepsilon < a_1 \\ 0 & \varepsilon \ge a_1 \end{cases} \quad (1)$$

$$\mu_{A2}(\varepsilon) = \begin{cases} 1 - \frac{\varepsilon - a_1}{0.5 b_2} & |\varepsilon - a_2| \le 0.5 b_2 \\ 0 & |\varepsilon - a_2| \ge 0.5 b_2 \end{cases} \quad (2)$$

$$\mu_{A3}(\varepsilon) = \begin{cases} 0 & \varepsilon \le a_3 \\ \frac{\varepsilon - a_1}{b_1 - a_1} & a_3 < \varepsilon < b_3 \\ 1 & \varepsilon \ge b_3 \end{cases} \quad (3)$$

where the value of parameters (a_i, b_i) changes with the change in error and accordingly generates the linguistic value of each membership function. Parameters in this layer are referred as premise parameters or precondition parameters.

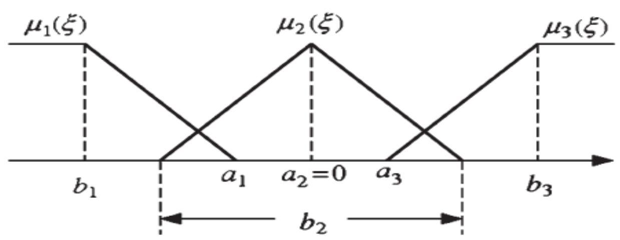


Figure.6 Fuzzy membership functions.

Layer 2: Every node in this layer is a circle labelled as Π. which multiplies the incoming signals and forwards it to next layer.

$\mu_i = \mu_{Ai}(\varepsilon_1).\mu_{Bi}(\varepsilon_2) \dots\dots$ i= 1, 2, 3. (4)

But in our case there is only one input, so this layer can be ignored and the output of first layer will directly pass to the third layer. Here, the output of each node represents the firing strength of a rule.

Layer 3: Every node in this layer is represented as circle. This layer calculates the normalized firing strength of each rule as given below:

$$\bar{\mu_i} = \frac{\mu_i}{\mu_1 + \mu_2 + \mu_3} \quad (5)$$

Layer 4: Every node in this layer is a node function

$$O_i = \bar{\mu_i}.f_i = \bar{\mu_i}(a_0^i + a_1^i \varepsilon) \text{ i=1,2,3.} \quad (6)$$

where the parameters (a_0^i, a_1^i)are tuned as the function of input (ξ). The parameters inthis layer are also referred as consequent parameters.

Layer 5: This layer is also called output layer which computes the output as given below:

$$Y = \overline{\mu_1}.f_1 + \overline{\mu_2}.f_2 + \overline{\mu_3}.f_3 \quad (7)$$

The output from this layer is multiplied with the normalizing factor to obtain the active power current component (i_d*').

IV MATLAB SIMULATION RESULTS

The proposed voltage control calculation is done in sundry conditions (i.e., stack step change, lopsided load, and nonlinear load) to faultlessly uncover its benefits. With a specific end goal to immediately connect with and separate the heap amid a transient condition, the on–off switch is utilized as appeared in Fig. 3. The resistive load portrayed in Fig. 4(a) is connected under both the heap step change condition (i.e., 0%–100%) and the lopsided load condition (i.e., stage B opened) to test the power of the proposed conspire when the heap is all of a sudden disengaged.

In viable applications, the most commonplace resilience varieties of the channel inductance (Lf) and channel capacitance (Cf), which are used as a yield channel, are inside ±10%. To assist legitimize the vigor under parameter varieties, a 30% lessening in both Lf and Cf is proposed under all heap conditions, for example, stack step change, unequal load, and nonlinear load.

Fig. 5 demonstrates the reenactment aftereffects of the proposed control technique amid the heap step change. Additionally, Fig. 6 exhibits the near results acquired by utilizing the customary ANFISscheme under a similar condition. Solidly, the figures show the heap voltages It is vital to note that the heap current blunder waveform in the aftereffects of the ordinary ANFISmethod is excluded on the grounds that the ANFISscheme does not require stack current data. It can be seen in Fig. 5 that when the heap is all of a sudden transmuted, the heap yield voltage exhibits little twisting. Be that as it may, it speedily comes back to a relentless state condition in 1.0 ms, as appeared in in the simulation results in fig9.

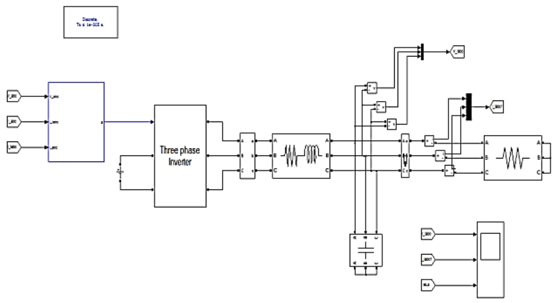


Fig.7Matlab/Simulink Model of the Proposed ANFIScontrol based UPS .

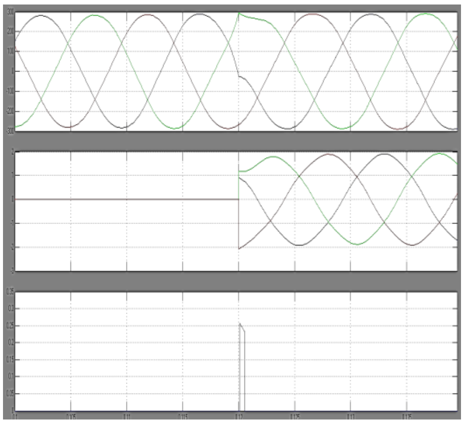


Fig.8 Simulation results Load Output Voltage (Vabcl), Load Output Current (Iabcl) & Error Current (Ie) under Linear load Condition.

Moreover, it has revealed a resilient instauration time of 1.5 ms in an authentic experimental setup as shown in Fig. 5(b). Conversely, as illustrated in the simulation results in Fig. 6(a), voltage distortion is more immensely colossal, and its instauration time of 1.4 ms is much longer as compared with that in Fig. 5(a). Moreover, Fig. 6(b) shows a longer recuperation time of 2.0 ms than that observed in Fig. 5(b).

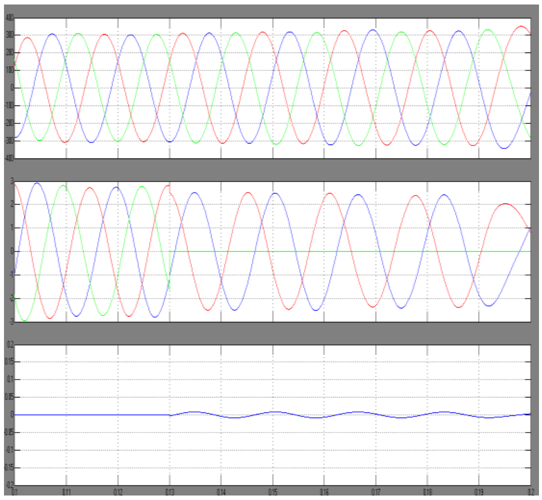


Fig.9 Simulation results Load Output Voltage (Vabcl), Load Output Current (Iabcl) & Error Current (Ie) under Linear Unbalanced load Condition.

On the other hand, the THD values of the load output voltage at steady-state full-load operation are presented in Table II. These values are found as 0.11% for simulation and 0.89% for experiment utilizing the proposed scheme. However, the conventional ANFISscheme shows 0.94% and 1.32% for the case of simulation and experiment, respectively. Ergo, it is explicitly demonstrated that the proposed algorithm procures lower THD. It can be observed from Table II that the load root mean square (RMS) voltage values in both schemes are opportunely regulated at steady state. Moreover, the third waveform in Fig. 5 shows a diminutive load.

Fig. 9. Recreation aftereffects of the ANFIS scheme under unequal load with −30% parameter varieties in Lf and Cf (i.e., stage B opened)— First: Load yield voltages (VL), Second: Load yield streams (IL). (a) Simulation. (b) Experiment. current blunder (ieLA) between the evaluated esteem (iLA) and the assessed esteem (ˆiLA). Next, the trademark exhibitions of the transient and relentless state under lopsided load are confirmed through Figs. 7 and 8. Exactly, this case is executed under a full-stack condition by all of a sudden opening stage B. It is demonstrated that the heap yield voltages are controlled well, but the quick transmutation in the heap current of stage B is seen as it is opened.

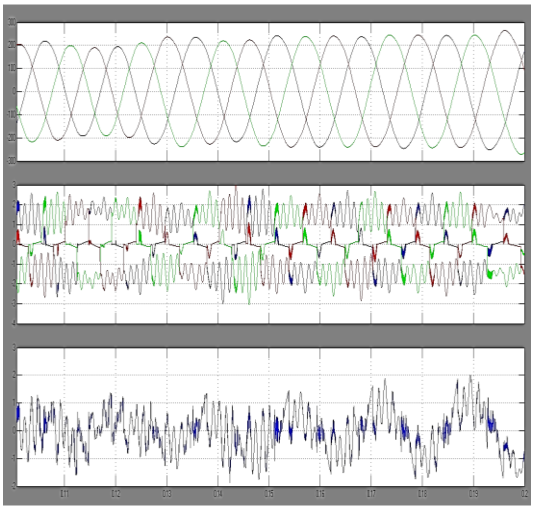


Fig.10 Simulation results Load Output Voltage (Vabcl), Load Output Current (Iabcl) & Error Current (Ie) under Non Linear load Condition.

As appeared in Fig. 7, the separate THD estimations of the yield voltage are 0.13% for the recreation and 0.91% for the examination acquired by using the proposed strategy. In any case, the THD qualities are 0.97% and 1.39%, separately, for the reproduction and examination if there should arise an occurrence of the routine ANFISscheme, as portrayed in Fig. 8. As given in Table II, little enduring state voltage blunders under lopsided load are watched on the grounds that the heap RMS voltage estimations of both techniques are practically 110 V.

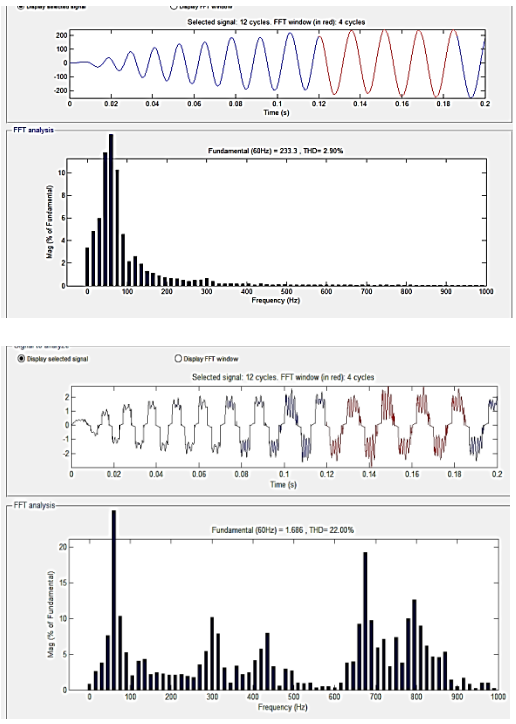


Fig11. THD Values of Input Current & Load current in %

In incorporation, the heap current eyewitness gives brilliant data to the proposed controller as depicted in Fig. 7. To assess the enduring state execution under nonlinear load, a three-stage diode rectifier appeared in Fig. 4(b) is used. The reenactment and trial consequences of every control strategy under this condition are exhibited in Figs. 9 and 10. To this end, the THD estimations of the heap voltage waveforms accomplished.

V CONCLUSION

This project has proposed a basic onlooker predicated ideal voltage control strategy for the three-stage UPS frameworks the proposed ANFIScontroller is made out of a criticism control term to settle the mistake progression of the framework and a repaying control term to appraise the framework vulnerabilities. Also, the ideal load current onlooker was accustomed to upgrade framework cost and unwavering quality. This paper demonstrated the shut circle strength of an eyewitness predicated ideal voltage controller by using the Lyapunov hypothesis. Moreover, the proposed voltage control law can be systematically outlined considering a tradeoff between control input extents and following mistake not at all like foremost calculations. The prevalent execution of the proposed control framework was exhibited through reproductions. Under three load conditions (stack step change, unequal load, and nonlinear load), the proposed control conspire uncovered a superior voltage following execution, for example, bring down THD, more infinitesimal unfaltering state blunder, and more speedy transient replication than the ordinary PI plot regardless of the possibility that there subsist parameter varieties.

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