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Survey of Logical Gates Family

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Abstract - *Logical gates are the basic building block of the any intelligence or processing device. It realizes the various logical operations and also supports the arithmetic operations. This is the essential requirement of any computing device this paper provide functionality and various aspects related to the logic gates family.*

Key Words: AND, OR, NOT, NAND, NOR, universal gates

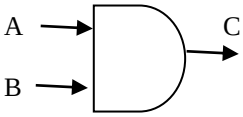
1.INTRODUCTION

Processor is a unit which take input from input device process it and generate the output. Processing logic can be of many types depending on the application or the user requirements. General purpose processor has generic logic while application oriented or specific processor have their own logic. The variety of inputs mechanism may be via keyboard, mouse, and controller sensors or via user interface. Output may be in form of commands, signals, to drivers which control the automated or generic process. Memory is an very important part which require to store the processor's logic or input and/or output data. Processor has no natural sense like human so it's responsibility of it's manufacturer or designer to put artificial intelligence in it. Such intelligence can be achieved through developing logic in processor.Processor perform action depending on such logic and process input data. Such logic can be achieved through use of single and/or multiple logic gates.

Functioning of Logical Gates

There are basically two main gate one perform logical ANDing or multiplication so it called AND and second do logical ORing or addition so called OR gate.

1) Logical Symbol of AND gate

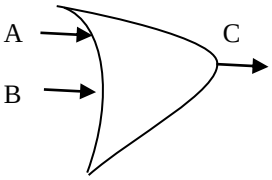


Truth Table

Inputs		Output
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

From the above truth table we can conclude that when any input is Low(0) the output of AND gate is Low(0)and when all the inputs are High(1) the output of AND gate is High(1) as this AND gate perform logical ANDing means Multiplication.

2) Logical Symbol of OR gate

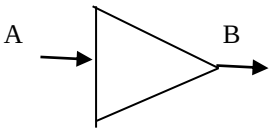


Truth Table

Inputs		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

From the above truth table we can conclude that when any input is High(1) the output of OR gate is High(1) Low(0)and when all the inputs are Low(0) the output of OR gate is Low(0) as this OR gate perform logical ORing mean Addition or summation.

3) Logical Symbol of Buffer gate

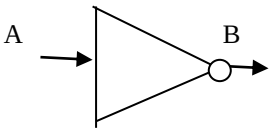


Truth Table

Inputs	Output
A	B
0	0
1	1

From the above truth table we can conclude that when input is High(1) the output of buffer gate is High(1)and when the input is Low(0)the output of buffer gate is also Low(0) .

4) Logical Symbol of NOT gate



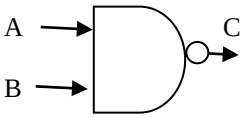
Truth Table

Input	Output
A	B
0	1
1	0

From the above truth table we can conclude that when input is High(1) the output of NOT gate is Low(0) and when the input is Low(0)the output of NOT gate is High(1) .

By Combing invert or bubble logic with AND and OR two universal gates NAND and NOR can be achieved as NOT +AND =NAND and NOT +OR =NOR. These two gates are called universal as any logic gates can be formulated with help of it.

5) Logical Symbol of NAND gate



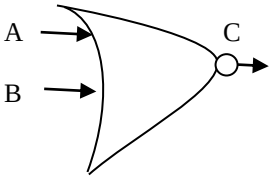
Truth Table

Inputs		Output
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

Bubbled NAND is equivalent to OR gate or Bubbled AND is equivalent to NOR gate such logic can be realized also with Demorgan's rule (A ◯ B)' =A' + B'

From the above truth table we can conclude that when all the input are High(1) the output of NAND gate is High(1) else Low(0) .

6) Logical Symbol of NOR gate

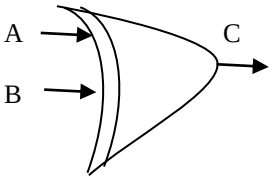


Truth Table

Inputs		Output
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

From the above truth table we can conclude that when all the inputs are Low (0) the output of NOR gate is High(1) else Low(0).

7) Logical Symbol of XOR gate

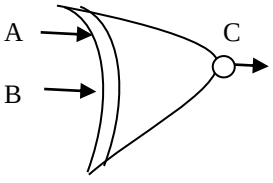


Truth Table

Inputs		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

From the above truth table we can conclude that when all the inputs are same either Low(0) or High(1) the output of XOR gate is Low(0) else High(1).

8) Logical Symbol of X-NOR gate

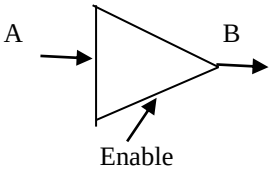


Truth Table

Inputs		Output
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

From the truth table we can conclude that when all the inputs are same either Low(0) or High(1) the output of X-NOR gate is High(1) else Low(0) .

9) Logical Symbol of Tri state Buffer gate



Truth Table

Inputs		Output
A	E	B
0/1	0	no o/p
0/1	1	0/1

From the above truth table we can conclude that when the enable input is High(1) we can get the output whatever the input else gate produce high impedance state in which no output is produce.

If we take 2 inputs as general model than implementation of above logic families with particular IC as given below each logic family is designed such that other logic family can be easily combined serve as basic building block and can produce into larger complex logic circuit with minimum additional components which is very much desirable property in any circuit design.

2. DESIGN PARAMETERS OF CIRCUIT

1) Cost: Manufacturing and end user cost should be minimum

2) Power requirement: the power need of any circuit or device also minimum that can be achieve through either using low power components or circuit or make power dissipation minimum

3) Size: The size of circuit or device should be minimum which also reduce its weight this can be achieved through high level of integration. Initially up to 10 transistors are integrated on chip so it called SSI(Small Scale Integration) they were very crucial in early computers then up to 100 transistors it called MSI(Medium Scale Integration).MSI were attractive economically because which they cost little more systems to be produced using smaller circuit boards, less assembly work, and a number of other advantages.

Next development was of Large Scale Integration (LSI). The development of LSI was driven by economic factors and each chip comprised tens of thousands of transistors. It was in 1970s, when LSI started getting manufactured in huge quantities.

LSI was followed by Very Large Scale Integration (VLSI) where hundreds of thousands of transistors were used and still being developed. It was for the first time that a CPU was fabricated on a single integrated circuit, to create a microprocessor. In 1986, with the introduction of first one

megabit RAM chips, more than one million transistors were integrated.

Microprocessor chips produced in 1994 contained more than three million transistors. ULSI refer to "Ultra-Large Scale Integration" and correspond to more than 1 million of transistors. However there is no qualitative leap between VLSI and ULSI, hence normally in technical texts the "VLSI" term cover ULSI.

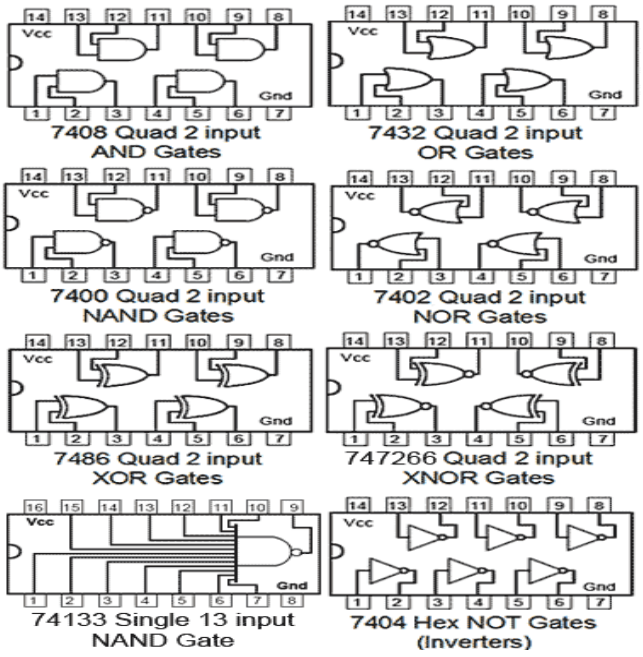


Fig -1: Various Gates Implementations

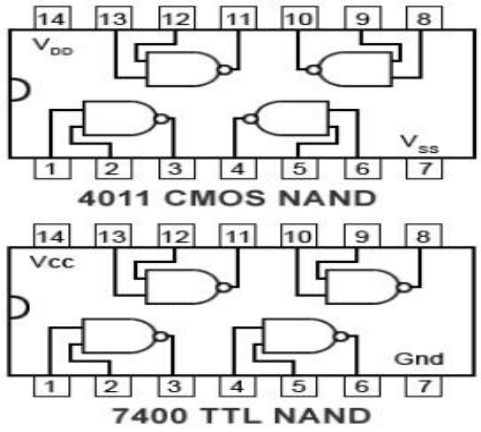


Fig -2: Original CMOS and TTL Pinouts for NAND gate IC

3. TERMINOLOGY ASSOSIATED WITH GATES

1) Power Dissipation (Pd): it is the requirement of power for the functioning of the gate it measured in milli-Watts(mW).

2) Propogation Delay(pd):it is the time required to change in output of the gate due to change in input it is measured in nano-second(ns)

3) Noise-Margin(Nm):It is the level of white noise at which gate can operate at normal functionality.

4) Fan out: It is the capability of the logic gate to drive the maximum number of similar gates.

5) Fan-In: is the number of inputs to a particular gate.

6) Figure of merit: The requirement of power to operate a gate which we called as Power Dissipation should be minimum to save the power but when it is reduced the speed of operation gets reduced, so Figure of merit is a tradeoff between them it is defined as product of propogation delay and Power dissipation. Figure of merit = Pd x pd unit is pJ (picco-Jule)

Table -1: Relationship between Boolean algebra and logical Gates

sr	Boolean function	symbol	Name	Output
1	F0=0		Null	reset
2	F1=xy	x*y	AND	X and y
3	F2=xy'	x/y	Inhibition	X,but not y
4	F3=x		transfer x	x
5	F4=x'y	y/x	Inhibition	y,but not x
6	F5=y		transfer y	y
7	F6=xy'+x'y	x xor y	Exclusive-OR	x or y,but not both
8	F7=x + y	X or y	OR	X or Y
9	F8=(x + y)'	X nor y	NOR	Not-OR
10	F9=xy +x'y'	(x xor y)'	equivalence	X equal y
11	F10=x'	X'	NOT x	Complement of x
12	F11= x + y'	X subset y	implication	If y then X
13	F12=y'	Y'	NOT y	Complement of y
14	F13 = x'+y	Y subset of x	implication	If x then y
15	F14=(x y)'	X nand y	NAND	Not-AND
16	F15=1		Identity	Set

From the above table we can realize that various arithmetic and logical operations can be accomplished with simple use of gates and its associated logic.

4. COMPARISION OF POWER AND SPPED

logic gates should be able to change state immediately and consume little or no power. However the laws of physics, as presently understood, say that this is not possible. All electrical circuits must consume some power, and any change in the voltages and currents in that circuit must take at least some time. Chip designers therefore had to try and reconcile the fact that higher speeds meant more power consumption, and so some families developed, using optimum speed whilst others were developed to use the minimum of power.so RTL(Resistor Transfer Logic),DTL(Diode Transistor Logic) and TTL(Transistor Transistor Logic) are supresed by CMOS (Complimentary Metal Oxide Semiconductor) chips, designed for minimum power, got faster and TTL families, using bipolar transistors for optimum speed, were developed that not only increased speed but also reduced power consumption.

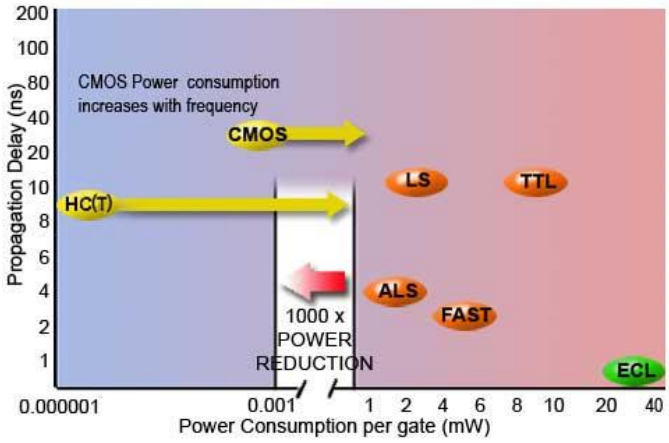


Fig -3: Power vs Speed relation

As the overall performance of these families increased they also became more compatible. The increase in portable (battery powered) electronic devices along with the ability of chip manufacturers to make the component parts of ICs much smaller also meant that power could be reduced and speed increased.

Some of the main TTL and CMOS sub-families currently in use are compared in Fig.6 Note how CMOS speed has been increased and power reduced with the introduction of the 74HC (High-speed CMOS) although (as the laws of physics demand), power consumption still increases, as the frequency at which they operate increases.

Because CMOS and TTL families can now operate at similar speeds and similar power consumption, the 74HCT (a CMOS sub-family compatible with TTL pinouts and voltage levels) now makes it possible to easily interface both families within in a single design, so enabling the use of the best features of each family.

74HC (and 74HCT for interfacing with the larger 74TTL families) are now recommended for most new designs.

The ECL (Emitter Coupled Logic) families, originated in the late 1950s and remain the fastest chips available, but consume more power, and because they use a negative power supply (of −5.2V) have been difficult to interface with other families. This has changed with the introduction of PECL (Positive ECL) using a +5V supply, and LVPECL (Low Voltage Positive ECL) using a +3.3V supply. This now offers the opportunity of using mixed CMOS and TTL families at various power levels for logic operations and interfacing with ECL for high frequency digital communications.

5. CONCLUSION

Each logic gate and logic family has unique electrical and electronics characteristic so they are unique and we can optimize them in circuit design by understanding their functionality and behavior.

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BIOGRAPHIES

Jiger Prakashchandra Acharya is Lecturer(ComputerDept.) Govt.Polytechnic –Ahmedabad.He has teaching experience of 15years.He has taken B.E.(EC) from North Gujarat University – PATAN in 2000 with First class and ME(EC_CSE) from GTU with 8.83 CPI in 2015.