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LOW POWER COMPARATOR USING DOUBLE TAIL GATE TECHNIQUE

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Abstract - *The need for low-power, are efficient, a high speed ADCs is pushing toward the use of dynamic reformative comparators to maximize speed and power efficiency. An analysis on the delay of the dynamic comparators will be presented and logical expressions are derived. From the investigative expressions, designers can obtain an intuition about the main donors to the comparator delay and fully explore the transactions in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a predictable double tail comparator is altered for low-power and fast operation even in small supply voltages. Without thwarting the design and by adding few transistors, the positive advice during the regeneration is reinforced, which results in remarkably reduced delay time. It is shown that in the proposed dynamic comparator both the power feasting and delay time are significantly reduced. The design and analysis is performed using 22 nm, 32 nm and 45 nm CMOS technology in Tanner EDA Tool*

Key Words: **Double-tail comparator, dynamic clocked comparator, high-speed analog-to-digital converters (ADCs), low-power analog design, Tanner EDA Tool**

1.INTRODUCTION

Comparators are mostly used in electronic components after operational amplifiers. Comparators are also known as 1-bit ADCs. So they are mostly used in large wealth in A/D converter. In the analog-to-digital conversion process, it is necessary to trial the input. This sampled signal is applied to comparators, to regulate the digital equivalent of the analog signal. In today's world, transferrable battery operator devices are increasing, because of low power policies are used for high speed applications. Power reduction can be realized by moving towards smaller size processes. However, as we move towards smaller feature size, these process disparities and other non-idealities will greatly affect the overall performance of the device. One such application where low power degeneracy, low noise, high speed, less hysteresis, less Offset voltage is required to Analog to Digital converters for mobile and portable devices. The precision of comparators is defined by its offset, along with power consumption, haste is of keen interest in achieving global higher performance of ADCs. In the past, pre-amplifier based comparators are used for ADC styles such as flash and pipeline. The main drawback of pre-amplifier based comparator is its offset voltage. To overcome these unruly, dynamic comparators are often used to make a judgement once every clock period and require much less offset voltage. However, these dynamic comparators are ached from large power dissipation compared to pre-amplifier based comparators. The main problem of these dynamic comparators is the output signal of latch stage is shifting during clock transition. This is happening due to the presence of noise at input terminals. The propose inverter based disparity amplifier topology eliminates the noise at input side. It also reduces the delay and power consumption.

2.Conventional Dynamic Comparator

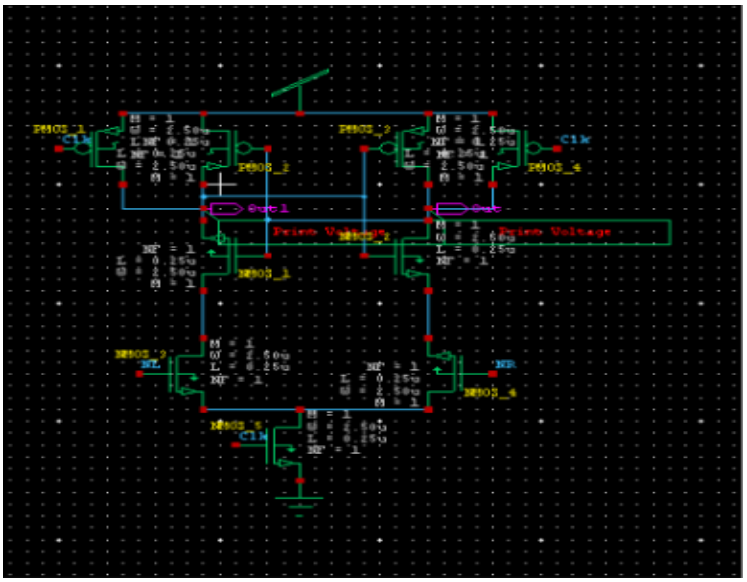

Fig. 1. Schematic diagram of the conservative dynamic comparator.

During the reset phase when CLK = 0 and *M*tail is off, reset transistors (*M*7–*M*8) tug both output nodes Out*n* and Out*p* to *V*DD to define a start condition and to have

a valid logical level during reset. In the comparison phase, when CLK = *V*DD, transistors *M*7 and *M*8 are off, and *M*tail is on. Output voltages (Out*p*, Out*n*), which had been pre-charged to *V*DD, start to discharge with different liquidating rates depending on the matching input voltage (INN/INP). Pretentious the case where *V*INP > *V*INN, Out*p* discharges faster than Out*n*, hence when Out*p* (discharged by transistor *M*2 drain current), falls down to *V*DD–|*V*thp| before Out*n* (discharged by transistor *M*1 drain current), the corresponding pMOS transistor (*M*5) will turn on initiating the latch revival caused by back-to-back inverters (*M*3, *M*5) and *M*4, *M*6). Thus, Out*n* pulls to *V*DD and Out*p* discharges to ground. If *V*INP < *V*INN, the circuits work vice versa. As shown in Fig. 2, the delay of this comparator is comprised of two time delays, *t*0 and *t*latch. The delay *t*0 represents the capacitive discharge of the load capacitance *C*L until
the first p-channel transistor (*M*5/*M*6) turns on. In case, the voltage at node INP is bigger than INN (i.e., *V*INP > *V*INN), the drain current of transistor *M*2 (*I*2) causes faster discharge of Out*p* node compared to the Out*n* node, which is driven by *M*1 with smaller current.

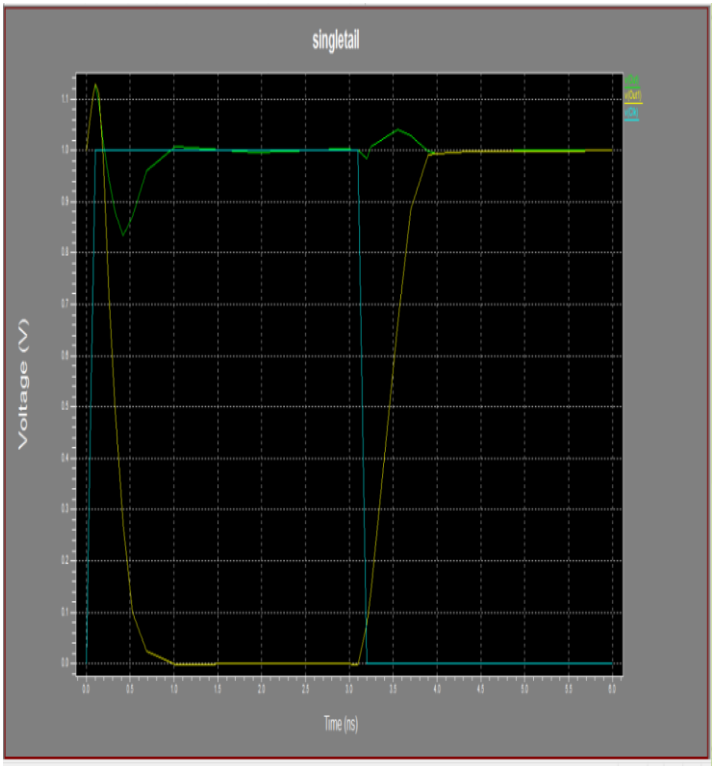

Fig. 2. Fleeting simulations of the conventional dynamic comparator for input voltage difference

3.Conventional Double-Tail Dynamic Comparator

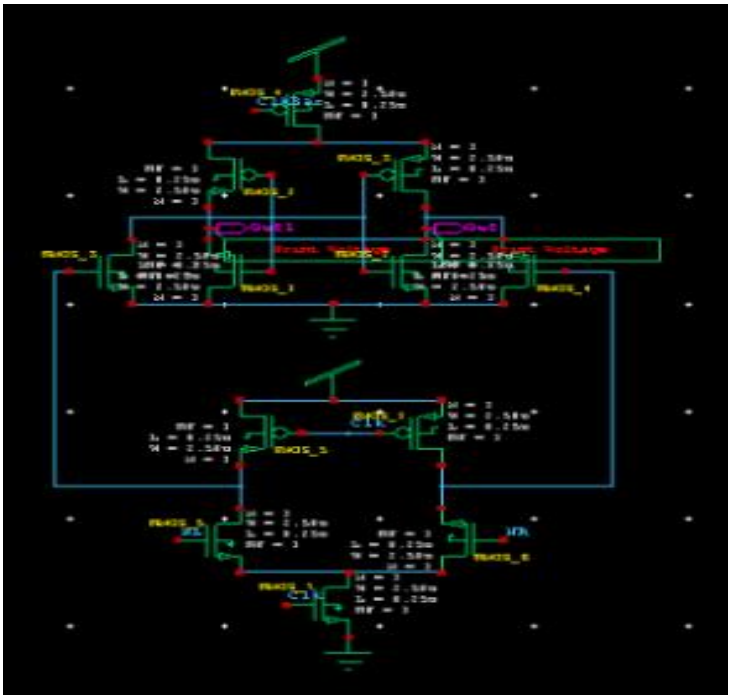

Fig. 3. Schematic diagram of the conservative double-tail dynamic comparator.

The dual tail enables both a large current in the latching stage and wider *M*tail2, for fast latching independent of the input common-mode voltage (*V*cm), and a small current in the input stage (small *M*tail1), for low offset [10]. During retune phase (CLK = 0, *M*tail1, and *M*tail2 are off), transistors *M*3-*M*4 pre-charge fn and fp nodes to *V*DD, which in turn causes transistors *M*R1 and *M*R2 to discharge the output nodes to ground. During executive phase (CLK =*V*DD, *M*tail1 and *M*tail2 turn on), *M*3-*M*4 turn off and voltages at nodes fn and fp start to drop with the rate defined by *I*Mtail1/*C*fn(p) and on top of this, an input-dependent differential voltage _*V*fn(p) will build up. The intermediate stage formed by *M*R1 and *M*R2 passes *V*fn(p) to the cross coupled inverters and also provides a good protecting between input and output, resulting in reduced value of reward noise [10]. Similar to the conventional dynamic comparator, the delay of this comparator comprises two main parts, *t*0 and *t*latch. The delay *t*0 represents the capacitive charging of the load capacitance *CL*out (at the latch stage output nodes, Out*n* and Out*p*) until the first n-channel transistor (*M*9/*M*10) turns on, after which the latch regeneration starts; thus *t*0 is obtained.

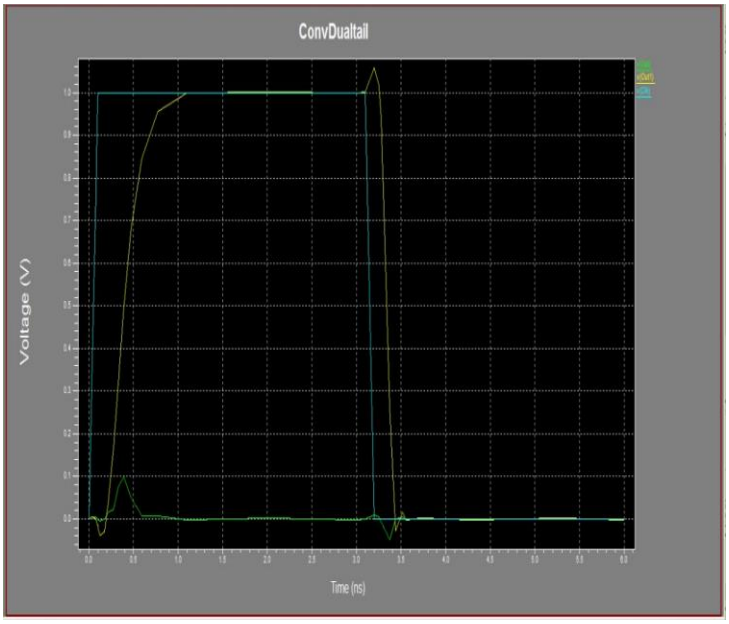

Fig. 4. Temporary simulations of the conventional double-tail dynamic comparator for input voltage difference.

During reset phase (CLK = 0, *M*tail1 and *M*tail2 are off, ducking static power), *M*3 and *M*4 pulls both fn and fp nodes to *V*DD, hence transistor *M*c1 and *M*c2 are cut off. Interim stage transistors, *M*R1 and *M*R2, reset both latch outputs to ground. During decision-making phase (CLK = *V*DD, *M*tail1, and *M*tail2 are on), transistors *M*3 and *M*4 turn off. Additionally, at the beginning of this phase, the control transistors are still off (since fn and fp are about *V*DD). Thus, fn and fp start to drop with different rates according to the input voltages. Suppose *V*INP > *V*INN, thus fn drops faster than fp, (since *M*2 provides more current than *M*1). As long as fn continues sinking, the agreeing pMOS control transistor (*M*c1 in this case) starts to turn on, pulling fp node back to the *V*DD; so another control transistor (*M*c2) remains off, allowing fn to be liquidated completely.

4. PROPOSED DOUBLE-TAIL DYNAMIC COMPARATOR

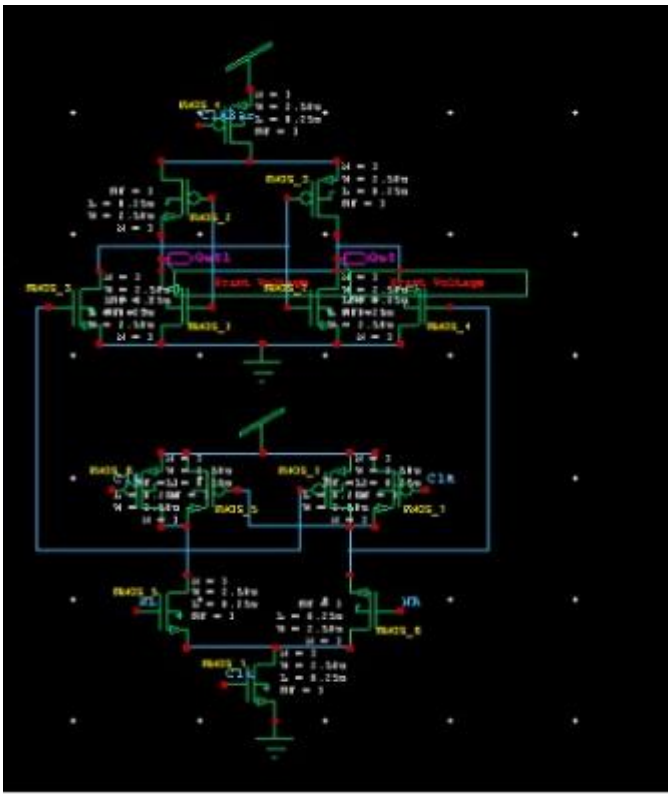

Fig. 5. Schematic diagram of the proposed dynamic comparator.

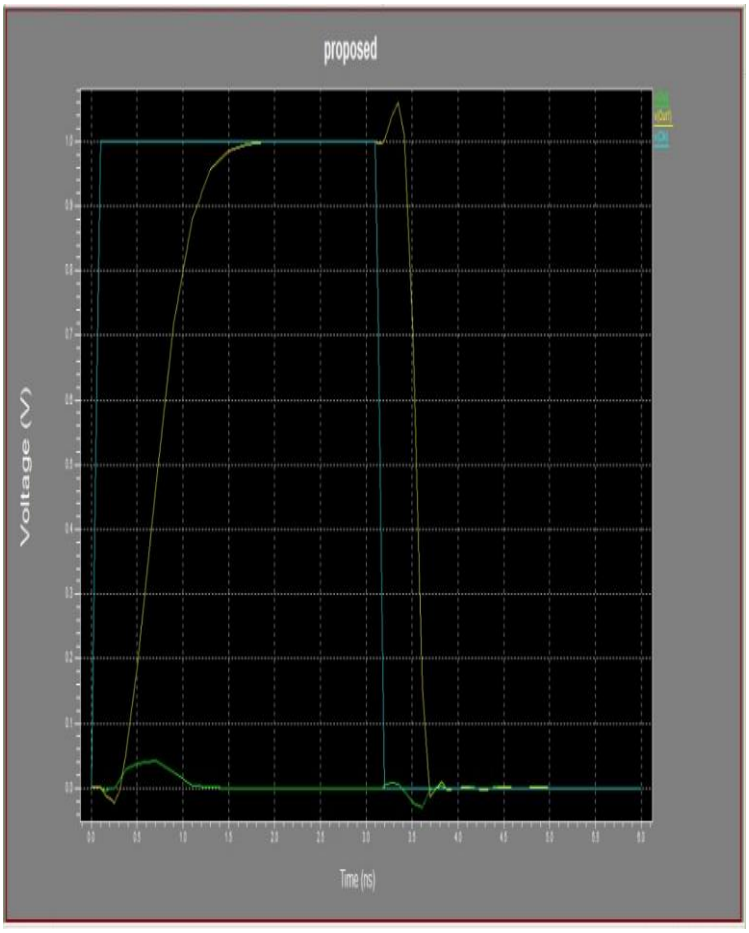

Fig. 6. Temporary simulations of the proposed double-tail dynamic comparator for input voltage difference

Table: Results

At 45nm	Power Dissipated	Delay
Single Tail Comparator	7.056 e-6W	1.245 e-5
Double Tail Comparator	8.872 e-11W	4.258 e-8
Proposed Comparator	5.496 e-11W	5.848 e-8

At 32nm	Power Dissipated	Delay
Single Tail Comparator	5.431 e-6W	4.257 e-6
Double Tail Comparator	4.790 e-11W	4.659 e-8
Proposed Comparator	5.961 e-13W	8.264 e-8

At 22nm	Power Dissipated	Delay
Single Tail Comparator	2.348 e-7W	2.367 e-7
Double Tail Comparator	8.628 e-11W	7.368 e-9
Proposed Comparator	7.127 e-13W	9.381 e-11

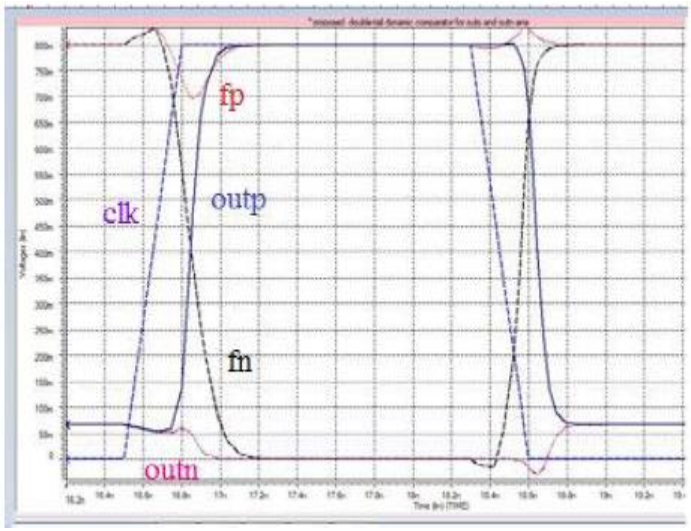

Chart -1 Simulation of Modified Double Tail Dynamic Comparator

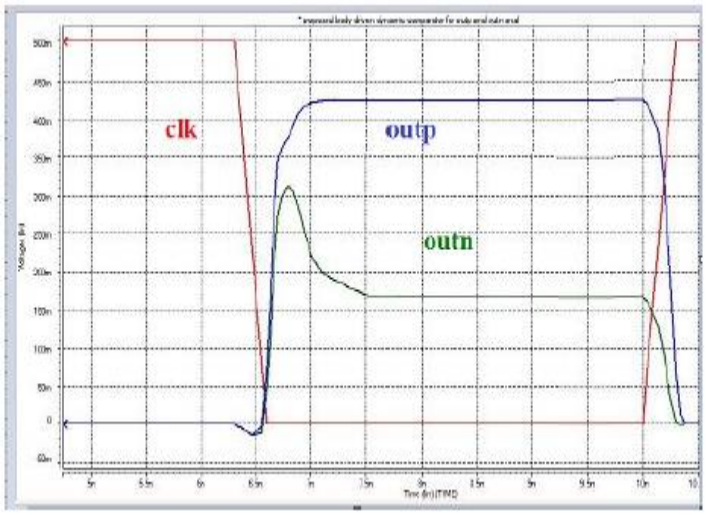

Chart -2 Simulation of proposed body driven Dynamic Comparator

3. CONCLUSIONS

In this paper, we presented a inclusive delay analysis for clocked dynamic comparators. Two common structures of conservative dynamic comparator and conventional double-tail dynamic comparators were investigated. A new dynamic comparator with low-voltage low-power ability was proposed in order to improve the performance of the comparator. Post-layout simulation results in 45nm, 32nm, 22nm CMOS technology confirmed that the delay and energy per adaptation of the proposed comparator is reduced to a great extent in comparison with the conventional dynamic comparator and double-tail comparator.

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BIOGRAPHIES

Sagar Sunil Pathak was born in Maharashtra, India. He received the B.E. degrees in Electronics and Telecommunication engineering from the North Maharashtra University of Maharashtra, India in 2014 and currently pursuing the M.Tech. degree, from the Department of Electronics Engineering and Technology, North Maharashtra University, Jalgaon in V.L.S.I. His current interests include low-power low-voltage analog and integrated circuits.