International Research Journal of Engineering and Technology (IRJET) e-ISSN: 2395 -0056
Volume: 03 Issue: 12 | Dec -2016 www.irjet.net p-ISSN: 2395-0072

PERFORMANCE ANALYSIS AND DESIGNING 16 BIT SRAM MEMORY CHIP USING XILINX TOOL

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Abstract - *In this paper a memory chip has been designed with the size of 16 bit using Xilinx software. For all those memory applications which requires high speed for example - in cache, SRAM is most often used. Xilinx ISE is an Electronic Design Automation (EDA) tool that allows integration in a single framework, different applications and tools (both proprietary and from other vendors), allowing to support all the stages of IC design and verification from a single environment. This tool is completely general, and supports different fabrication technologies. When we select a particular technology, a set of configuration and technology-related files are employed for customizing the Xilinx environment.*

Key Words: Electronic Design Automation (EDA), Static Random Access Memory (SRAM), Integrated Circuit (IC), Dynamic Random Access Memory (DRAM), VHSIC Hardware Description Language (VHDL)

1.INTRODUCTION

Fast low power SRAMs are becoming the critical component of many VLSI chips. There is increasing divergence in the speed of the processors and the main memory, and the power dissipation is also increasing due to increase in the integration and the operating speed as well as increase in the battery powered devices. The SRAM helps in bridging the gap and also reducing the power dissipation.

1.1 Why use a SRAM?

There are many reasons due to which we use an SRAM in a system design. Design tradeoffs will include density, speed, volatility, cost, and many other features. All these factors should be considered before selecting a RAM for designing our system. Let us discuss all these factors in brief:

• Speed
The primary and the foremost advantage of an SRAM over DRAM is its speed. The fastest DRAMs on the market still requires five to ten processor clock cycles to access the first bit of data.

• Density: DRAMs have significantly higher densities than the largest SRAMs because of the way DRAM and SRAM memory cells are designed.

• Volatility: The SRAM memory cells require more space on the silicon chip, but they have other advantages that translate directly into improved performance.
Unlike DRAMs, SRAM cells do not need to be refreshed. They are available for reading and writing data 100% of the time.

• Cost: If cost is the major factor in a memory design, then DRAMs will be the best to use instead of SRAM. If, on the other hand, performance is a critical factor then using a well-designed SRAM is an effective and cost performance solution for us.
• Custom features: Most DRAMs come in only one or two flavors or forms. Due to which the cost of them remains down, but this does not help when you need a particular kind of addressing sequence, or some other custom feature.

2. BASIC ARCHITECTURE

The general block diagram of a typical SRAM is shown in Figure 1 below. SRAM can be organized in two ways. It can be organized either as bit oriented or as word oriented. In the first case that is bit oriented SRAM, each address accesses a single bit, whereas in the other case that is word oriented memory, each address will access a word. The length of the word will be of n bits
The main SRAM building blocks include various components. All these components or blocks used in the SRAM are listed as follows:

- SRAM cell
- Pre-Charge Circuit
- Write Driver circuit
- Sense Amplifier
- Row decoder.

2.1 SRAM CELL

A Typical SRAM cell is made up of six MOSFETs. The number of these MOSFETs can vary. Each bit in an SRAM is stored on

four transistors named as (M1, M2, M3, and M4). These transistors form two cross – coupled inverters. This storage cell has two stable states which are denoted by 0 and 1. Other two additional access transistors are used to control the access to a storage cell during read and write operations. In addition to such six – transistor (6T) SRAM, other kinds of SRAM chips use 4, 8, 10 also called (4T, 8T, 10T SRAM), or more transistors per bit.

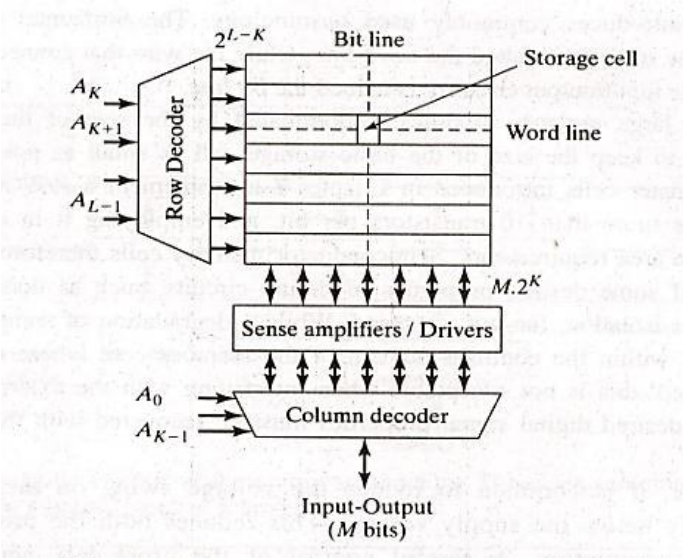

Fig- 1: SRAM Array Architecture

2.1.1 SRAM Cell Operation

An SRAM cell has three different states. These states are described in brief as below. It can be in:

- Standby (where the circuit is idle),
- Reading (in which the data has been requested) and
- Writing (helps in updating the contents).

2.2 PRECHARGE CIRCUIT

The pre-charge circuit is one of the vital components that are constantly used within SRAM cell. The aim of the pre-charge is to charge the bit and bit line bar to Vdd = 1.8v. As the name suggests, pre-charge is used for charging something or some devices. The pre-charge circuit sets the bit lines to be charged high at all times throughout the read and write operation.

2.3 DRIVER CIRCUIT

The driver circuit is one of the basic and important components in the memory design circuit. Its job is to bring the bit line and bit line bar to ground potential for the further job or operation. Before this the bit line and bit line are being charged maximum supply voltage Vdd through the pre-charge circuit

With pre-charge circuit it was get charged and after that it gets discharged with the help of the driver circuit. It is also known as write driver. The driver gets enabled by the word enable which is connected in the upper part of the circuit. The bit line which is close to the 0 logic will get discharged first, after that its logic gets inverted or complimented. In the similar manner the bit line and bit line bar gets discharged to the ground. With this kind of operation the bit line and bit line bar gets discharged.

2.4 SENSE AMPLIFIER

Sense amplifiers are the vital component in the memory designing process. The job of the sense amplifier is to sense the bit line and bit line bar for proper monitoring action. It improves the speed of the read and writes operation of the memory cell. It's another job or work is to reduce the power needed for the operation or we can say decrease the power consumption. The sense amplifiers major task is the amplification of the voltage difference which is being produced on the bit line and bit line bar at the time of operation.
Sense amplifiers play a major role in the functionality, performance and reliability of memory circuits.

2.4.1 Functions of sense amplifier

Following are the functions of the sense amplifier which are listed below:

1. Amplification
2. Delay Reduction
3. Power reduction

2.5 DECODER

Decoder is a combinational circuit that is used to convert the binary information from n input lines to a maximum of 2n unique outputs lines. Enable inputs must be on or it must be high for the decoder function; otherwise its outputs assume a single "disabled" output code word. By doing this the binary input conversion gets easier with the operation and we can get the desired output from this kind of combinational output. We can use these output lines for the number of operations like data, word line selection for the memory cell and also for the other digital information storage purpose.

3.SIMULATION RESULT

Reduction of power dissipation or power consumption in the memories is becoming of premier importance in the arena of digital design. Portable applications are lowering the bar on how much power memory may be consumed. The program written in the Xilinx ISE Webpack is shown in figure 2.

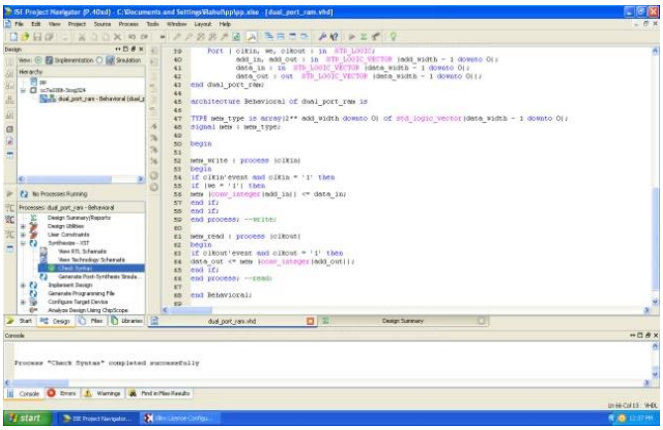

Fig- 2: Program written in Xilinx software

The program is written and the syntax is checked successfully. After this we have created RTL schematic. For this the software first asks for the selection of the elements. After selecting the elements we have to click on the tab Create Schematic. As soon as we click on this tab, we see the RTL schematic of the program.

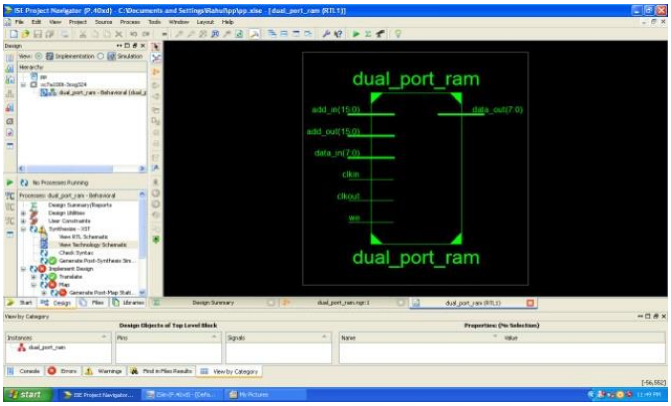

Fig- 3: RTL schematic in Xilinx software

After doing all this we will simulate the VHDL code using the ISim simulator. The waveforms of all the input and output parameters are displayed on the screen. We can then provide the input and observe the output.

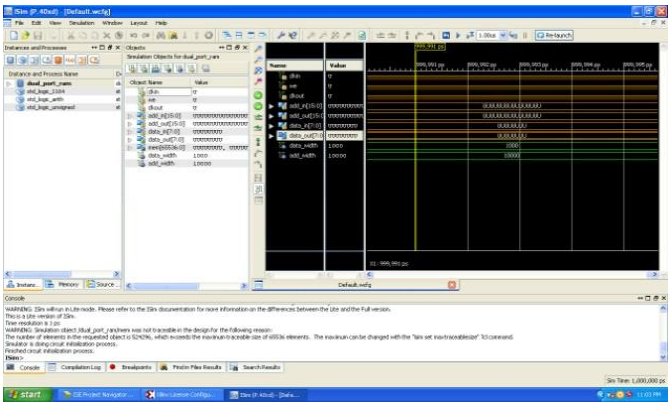

Figure 4: Waveform in Xilinx software

4.CONCLUSION

The simulated waveforms have shown that the architecture is an effective testing method to design embedded memories as it offers various advantages. In this project we have discussed about the simulation result that is being done for the above memory cell. The work is being carried out with Xilinx design software with read and writes operation in the above layout. We have designed a 16 bit memory cell with this software. The stop time of the cell is 10ns. The duration of write enable and sense enable set to 5ns. The pre-charge level is Vdd/2. The delay in the decoder circuit is 270 ps. For which we are getting the output that follows to the inputs but after some interval of time due to delay.

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