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POWER QUALITY ENHANCEMENT USING GRID INTERFACED DUAL VOLTAGE SOURCE INVERTER

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Abstract – *This paper demonstrates the functions of a dual voltage source inverter (DVSI) to improve power quality and reliability of the microgrid system using instantaneous symmetrical component theory (ISCT). The proposed DVSI scheme consists of two inverters named main voltage source inverter (MVSI) and auxilary voltage source inverter (AVSI) connected to the grid and load at the point of common coupling (PCC). Control algorithms are developed using ISCT to operate MVSI in grid injecting and grid sharing mode and AVSI in compensating reactive, harmonic and unbalanced components in load. Therefore, DVSI scheme has advantages like increase in reliability due to the decrease in failure rate of components and reduction in filter design.*

Key words: **Microgrid, voltage source inverter, instantaneous symmetrical component theory (ISCT), power quality.**

1. INTRODUCTION

Technology improvement and environment problems make the power system to a model which integrates distributed renewable energy resources to the grid called as micro grid [1]. Microgrid is a local energy system with renewable energy resources like PV or wind systems with energy storage facility. Generally power quality maintenance is one of the most important aspects in the power system. An inverter plays a vital role for power exchanging from microgrid to load [2]. Due to the presence of harmonics, unbalanced components and power electronic devices in the system, the voltages are distorted and decreases the power quality. But the manufacturing units, factories, industries etc. require clean power because they use high cost equipment. Therefore, it is necessary to compensate the unbalanced load components [3]. The compensation of unbalanced loads using voltage source inverter is discussed in the literature [4].

Power quality improvement using a single inverter system is discussed in [5]. This work presents the multifunctionalities of a single inverter for the distributed generation power system. In case of grid connected inverter, the inverter capacity for the utilization of load compensation is decided by available instantaneous real power. It shows that multifunctionalities in a single inverter either degrade real power exchange or the capability to compensate loads.

This paper explains a dual voltage source inverter, where the power generated from the microgrid is injected as real power by MVSI and unbalanced load compensation is performed by AVSI. If sufficient renewable power is available at the dc-link then the rated capacity of MVSI always inject real power to the grid. In DVSI, power loss across the switches of each inverter is reduced. As the main inverter is supplying real power, the inverter has to track the fundamental positive sequence components of current that results in reduction of main inverter bandwidth. Smaller size modular inverters operate at high switching frequencies with a small size interfacing inductor, so the cost of filter gets reduced. The control algorithm to operate DVSI in grid connected mode and to compensate nonlinear components is developed by using ISCT theory [9]. The dq0 transformation is used to extract the fundamental positive sequence components of PCC voltages.

2. DUAL VOLTAGE SOURCE INVERTER

2.1 System configuration

The proposed DVSI circuit is shown in fig.1. It consists of 2 inverters which are connected to the grid at point of common coupling and suppling unbalanced loads. A neutral point clamped (NPC) inverter is used as a auxilary voltage source inverter that compensates reactive, harmonic and unbalanced components in load currents. Capacitors C_1 and C_2 represents the split capacitor topology of dc-link of the AVSI. Five level inverter is used as the main voltage source

inverter that supplies the power generated from the distributed energy resources (DER) to grid. The DER can be either dc source or ac source. The load connected in this system is unbalanced and nonlinear load. The inverter is connected to the grid and load at the point of common coupling (PCC). Resistance (R_f) and inductance (L_f) represents the feeder impedance. Also $i_{g(abc)}$ represents grid currents, $i_{\mu gm(abc)}$ represents MVSI currents. $i_{\mu gx(abc)}$ represents AVSI currents, $i_{l(abc)}$ represents load currents, $v_{t(abc)}$ represents PCC voltages.

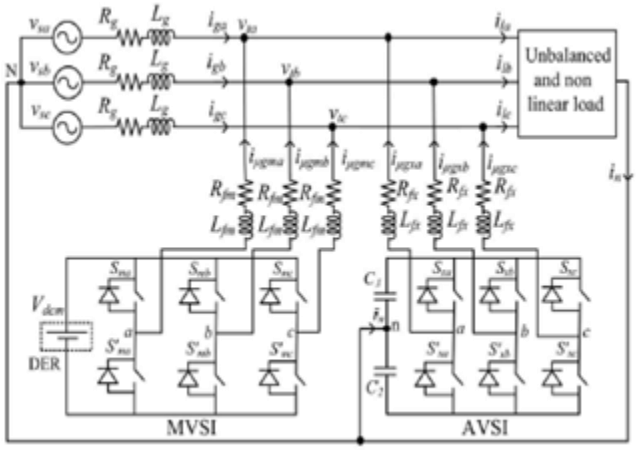

Fig.1. DVSI system configuration

2.2 Design of DVSI parameters

A. AVSI:

The parameters of the AVSI are dc-link voltage (v_{dc}), dc storage capacitors (C_1 and C_2), interfacing inductance L_{fx} and hysteresis band ($\pm h_x$). These are selected from the design method of split capacitor DSTATCOM model [6]. The voltage across each capacitor is taken as 1.6 times of peak value of phase voltage. Therefore total dc-link voltage (v_{dcr}), the sum of reference voltage across two capacitors v_{dc1} and v_{dc2} is calculated as 1040v.

Value of capacitors AVSI are taken from the change in dc-link voltage during transients. Consider S(kva) be the total load rating and the load power may vary from 0 to S(kva). To maintain load power demand AVSI need to transfer real power during transients. Hence, the exchange of maximum energy during transients equals the change in capacitor stored energy.

$$\frac{1}{2}C_1(V_{dc1}^2 - V_{dc2}^2) = nST \qquad (1)$$

Where V_{dcr}= 520v, V_{dc1}=0.8*V_{dcr}, n=1(number of cycles), T=0.02s(system time period), S=6kva. By substituting above values in eq(1), the capacitance (C_1) value is calculated as 2000μF. Sam value is taken for C_2. The interfacing inductance is calculated as

$$L_{fx} = \frac{1.6V_m}{4h_x f_{max}} \qquad (2)$$

Where f_{max} = 10kHz and h_x = 5% of load current.

A. MVSI

A five level inverter is used as a MVSI. Power generated from DER such as PV or wind energy system is coupled to dc link of the inverter. The dc-link voltage is taken as 1.15*V_{ml} where V_{ml} is the peak value of line voltage. At unity factor MVSI supplies a balanced sinusoidal current, so zero switching harmonics are absent in the output current of MVSI. Thus filter requirement for MVSI reduced.

3. CONTROLLING OF DVSI SCHEME

3.1 Extraction of fundamental voltage

The ISCT algorithm requires balanced sinusoidal PCC voltages for the generation of reference filter currents. Due to the feeder impedance at the source, the harmonic components distort the voltages at point of common coupling. Therefore, the fundamental positive sequences of PCC voltages are extracted for the generation of reference filter currents. These distorted PCC voltages must be converted to balanced sinusoidal voltages by using dq0 transformation [7].

In dq0 transformation, first the PCC voltages (v_{ta},v_{tb},v_{tc}) are transformed to dq0 reference voltages as given below

$$\begin{bmatrix} v_{td} \\ v_{tq} \\ v_{t0} \end{bmatrix} = C \begin{bmatrix} v_{ta} \\ v_{tb} \\ v_{tc} \end{bmatrix} \qquad (3)$$

Where

$$C = \sqrt{\frac{2}{3}} \begin{bmatrix} \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

The matrix[C] is solved by using θ value. This θ value is obtained from the synchronous reference frame (SRF) phase locked loop (PLL) [9]. Fig.2 represents the block diagram of PLL. In PLL, the synchronous reference frame voltage (v_{tq}) in q-axis is compared with 0v and the obtained error voltage is

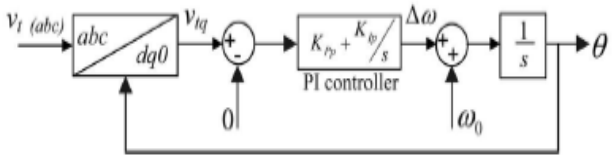

Fig.2. Block diagram of PLL

given to the PI controller. From the PI controller, frequency deviation (Δω) is calculated using K_p and K_I values. The frequency deviation (Δω) is added to the reference frequency(ω_0), the resultant ($\omega_0 + \Delta\omega$) is finally given to the integrator to calculate θ value. Using park's transformation matrix(C) at θ=$\omega_0 t$, voltage at q-axis in dq0 frame becomes zero. Hence, the PLL will be locked to the reference frequency(ω_0). The transformed voltages(V_{td} and V_{tq}) contain oscillating and average components of voltages.

$$v_{td} = \bar{v}_{td} + \tilde{v}_{td}$$

$$v_{tq} = \bar{v}_{tq} + \tilde{v}_{tq} \quad (4)$$

Where $\bar{v}_{td}$ *and* $\bar{v}_{tq}$ represent the average components and $\tilde{v}_{td}$ *and* $\tilde{v}_{tq}$represent the oscillating components. By applying inverse dq0 transformation technique to dq0 reference frame voltages, the fundamental positive sequence of PCC voltages in natural reference frame are obtained as given below

$$\begin{bmatrix} v_{ta}^{+} \\ v_{tb}^{+} \\ v_{tc}^{+} \end{bmatrix} = C^{T} \begin{bmatrix} \bar{v}_{td} \\ \bar{v}_{tq} \\ 0 \end{bmatrix} \quad (5)$$

The positive sequence voltages ($v_{ta1}^{+}, v_{tb1}^{+}, v_{tc1}^{+}$) are used for the ISCT algorithm, to draw balanced sinusoidal currents.

3.2 Instantaneous symmetrical component theory

ISCT was used primarily for the nonlinear and unbalanced load compensation by active filters.

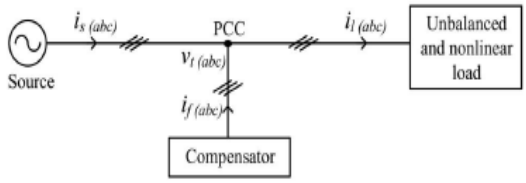

Fig.3. Block diagram of unbalanced and non-linear load compensation scheme

The block diagram shown in fig.3 is used for generating the reference current for the compensator. The ISCT for load compensation is developed by using three conditions given below

1. The source neutral current must be zero.
$$i_{sa} + i_{sb} + i_{sc} = 0 \quad (6)$$
2. The term ϕ is the phase angle between source current (i_{sa}) and the fundamental positive sequence voltage (v_{ta1}^{+}).
$$\angle v_{ta1}^{+} = \angle i_{sa} + \phi \quad (7)$$
3. The average load real power (P_l) should be supplied by the source.
$$v_{ta1}^{+} i_{sa} + v_{tb1}^{+} i_{sb} + v_{tc1}^{+} i_{sc} = P_l \quad (8)$$

By solving above three equations, the reference source currents are obtained as

$$i_{sa}^{*} = \left(\frac{v_{ta1}^{+} + \beta(v_{tb1}^{+} - v_{tc1}^{+})}{\sum j=a,b,c v_{tj}^{+2}}\right) P_l$$

$$i_{sb}^{*} = \left(\frac{v_{tb1}^{+} + \beta(v_{tc1}^{+} - v_{tb1}^{+})}{\sum j=a,b,c v_{tj}^{+2}}\right) P_l$$

$$i_{sc}^{*} = \left(\frac{v_{tc1}^{+} + \beta(v_{ta1}^{+} - v_{tb1}^{+})}{\sum j=a,b,c v_{tj}^{+2}}\right) P_l \quad (9)$$

Where $\beta = \frac{\tan\phi}{\sqrt{3}}$. The term ϕ is the phase angle between the source current and the fundamental positive sequence of PCC voltages. By substituting β=0 in eq(9), the unity power factor for the source current is achieved. Therefore, the reference source current for three phases are given by

$$i_{s(abc)}^{*} = \left(\frac{v_{t(abc)1}^{+}}{\sum j=a,b,c v_{tj}^{+2}}\right) P_l \quad (10)$$

The average load power(P_l) can be calculated by using a moving average filter with a window of one-cycle data points as shown below

$$P_l = \frac{1}{T}\int_{t_1-T}^{t_1} (v_{ta1}^{+} i_{la} + v_{tb1}^{+} i_{lb} + v_{tc1}^{+} i_{lc}) dt \quad (11)$$

Where t_1 is any arbitrary time constant. Finally, the reference currents for the compensator are generated using the below equation.

$$i_{f(abc)}^{*} = i_{l(abc)} - i_{s(abc)}^{*} \quad (12)$$

When the total load active power (P_l) is supplied by the source, the reference filter currents are generated by using

the equation (12). A modification in the control algorithm is needed for the DVSI scheme, i.e., source currents $i_{s(abc)}$represents grid currents $i_{g(abc)}$ and filter currents $i_{f(abc)}$represents AVSI currents $i_{\mu gx(abc)}$.

3.3 Control method of DVSI

The control method of DVSI explains the grid sharing and grid injecting mode and also compensation method by AVSI.

3.3.1 Generation of reference current for auxiliary inverter:

For the proper operation of auxiliary inverter, DC-link voltage changes due to the switching and ohmic losses (P_{loss}) that is supplied by the grid. An expression for P_{loss} is derived from the condition that average dc capacitor current is zero to maintain a constant capacitor voltage. A change in capacitor voltage from a steady state value occurs due to the deviation of average capacitor current from zero. A PI controller is used to generate P_{loss} as shown below.

$$P_{loss}=K_{Pv}e_{vdc} + K_{Iv}\int e_{vdc}\,dt \qquad (13)$$

Where $e_{vdc} = V_{dcref} - v_{dc}$, v_{dc} is the actual voltage sensed. K_{Pv} and K_{Iv} represent proportional and integral gains of PI controller. Therefore, AVSI reference currents can be obtained from equation (14)

$$i^{*}_{\mu gx(abc)} = i_{l(abc)} - \left(\frac{v^{+}_{t(abc)1}}{\sum j=a,b,c v^{+2}_{tj}}\right)(P_l - P_{loss}) \qquad (14)$$

3.3.2 Generation of reference current for MVSI:

The MVSI supplies balanced sinusoidal currents depend on the available power at DER. The power injected to the grid will be equal to the power available at DER ($P_{\mu g}$) when MVSI losses are neglected. The reference currents of MVSI for three phases are generated from the below equation

$$i^{*}_{\mu gm(abc)} = \left(\frac{v^{+}_{t(abc)1}}{\sum j=a,b,c v^{+2}_{tj}}\right)P_{\mu g} \qquad (15)$$

Where $P_{\mu g}$ is the available power at the dc-link of MVSI.

The reference currents generated from (14) and (15) are tracked by using hysteresis band current controller (HBCC). HBCC uses a feedback loop, usually a two-level comparator. A hysteresis current controller is a high gain proportional controller that adds certain phase lag in the operation based on the hysteresis band and does not the system unstable. A first order inductor filter is used that retains the closed loop system stability. The total controlling diagram of DVSI method is shown in fig.4. Applying Kirchhoff's current law(KCL) at the PCC

$$i_{\mu gxj} = i_{lj} - (i_{gj} + i_{\mu gmj})$$

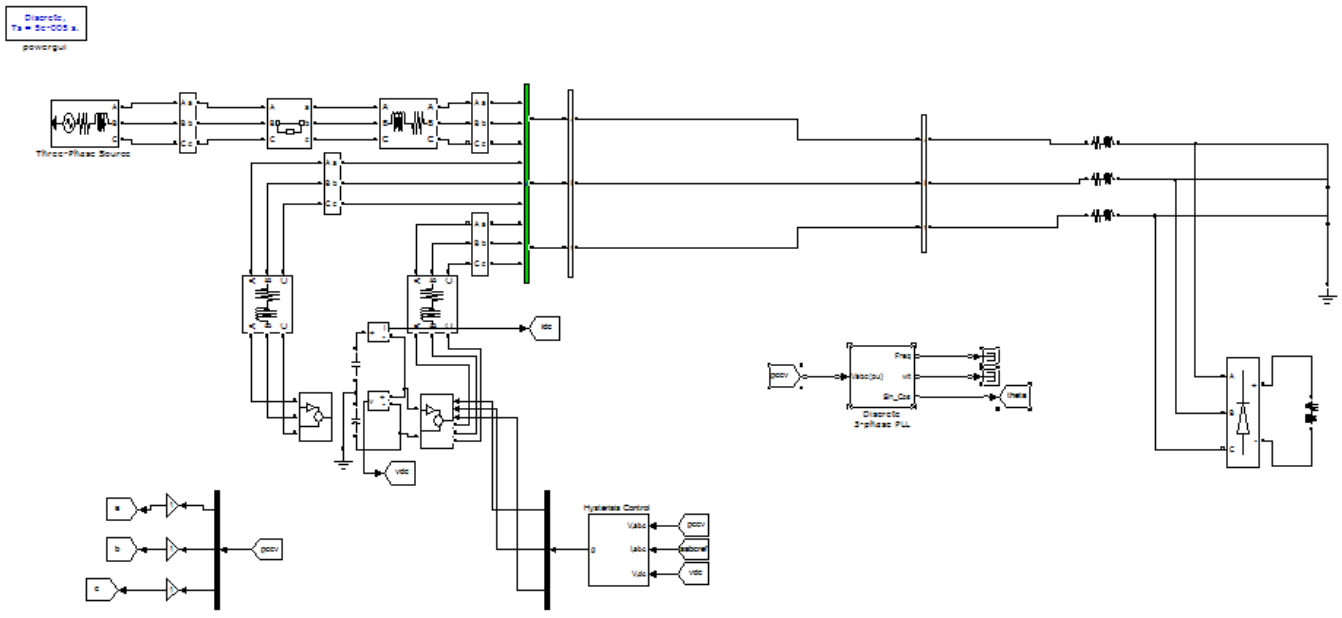

Fig.4. Control diagram of DVSI scheme

By using (14) and (16), reference grid current expression in phase (a) is obtained as

$$i_{ga}^{*} = \left(\frac{v_{ta1}^{+}}{\sum_{j=a,b,c} v_{tj}^{+2}}\right)\left[(P_l + P_{loss}) - P_{\mu g}\right] \qquad (16)$$

If the quantity (P_l+P_{loss}) is greater than $P_{\mu g}$, the term [(P_l+P_{loss})-$P_{\mu g}$] will be a positive quantity and i_{ga}^{*} is in phase with v_{ta1}^{+}. This operation is called as the grid supporting mode. Here the total load power is shared between MVSI and grid. If (P_l+P_{loss}) is less than $P_{\mu g}$, then [(P_l+P_{loss})-$P_{\mu g}$] will be a negative quantity and i_{ga}^{*} is in phase opposition with v_{ta1}^{+}. This is called as the grid injecting mode. Here the excess power is injected to the grid.

4. SIMULATION RESULTS

The simulation model of DVSI method is developed in MATLAB 7.12.0 to evaluate the performance. The simulation results explains the grid sharing and grid injecting modes of operation of DVSI method in steady state as well as in transient condition and also unbalanced load compensation technique by AVSI. The voltages at the point of common coupling are distorted due to the feeder impedance. If these distorted voltages are used for the generation of reference current of AVSI, the compensation of unbalanced components in load currents is not proper. Therefore, balanced sinusoidal voltages are required for the reference current generation.

The fundamental positive sequence voltages are extracted from the distorted voltages using ISCT algorithm. Fig.5(a) shows the fundamental positive sequence of PCC voltages.

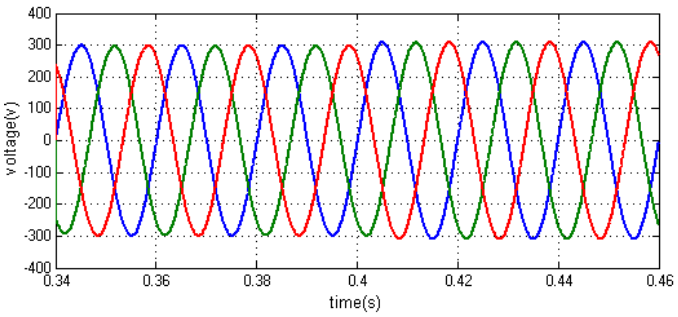

Fig.5. fundamental positive sequence of PCC voltages

Fig.6(a)-6(d) represents active power demanded by the load (P_l), active power supplied by the grid (P_g), active power supplied by the MVSI ($P_{\mu g}$), active power supplied by the AVSI (P_x). It is observed that, from t=0.1 to 0.4s MVSI is

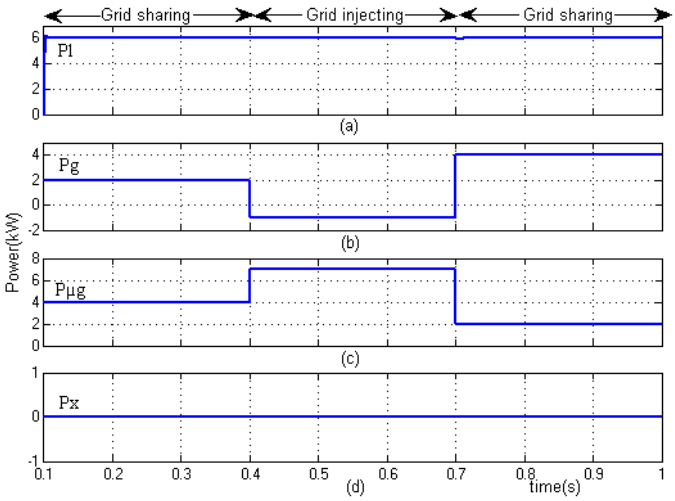

Fig.6. Active power sharing: (a) load active power; (b) active power supplied by grid; (c) active power supplied by MVSI; (d) active power supplied by AVSI

generating 4kW power but the load demand is 6kW. Therefore, the remaining load active power (2kW) is drawn from the grid. This period is called grid sharing mode. At t=0.4s the power generated from DER is increased to 7kW, which is more than the load demand (6kW). Therefore, the excess power(1kW) is injected to the grid. This is called as grid injecting mode.

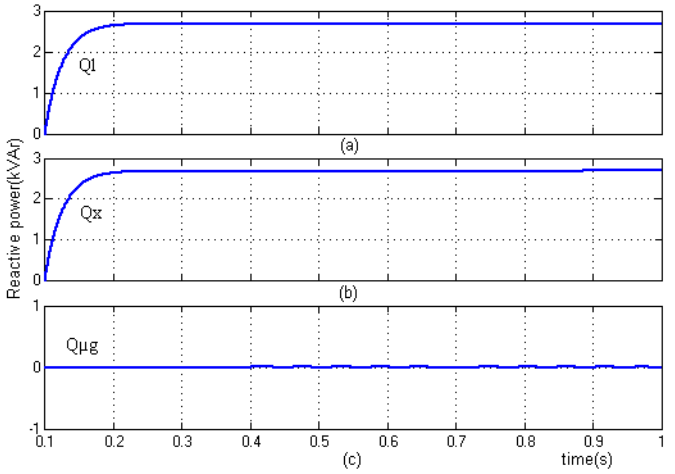

Fig.7. Reactive power sharing: (a) load reactive power; (b) reactive power supplied by AVSI; (c) reactive power supplied by MVSI.

Fig.7(a)-7(c) shows the load reactive power (Q_l), reactive power supplied by AVSI, and reactive power supplied by MVSI. It shows that total load reactive power is supplied by AVSI and MVSI does not supply reactive power.

Fig.8(a)-8(d) represents the plots of load currents $i_{l(abc)}$, currents drawn from the grid $i_{g(abc)}$, currents drawn from MVSI $i_{\mu g(abc)}$, currents drawn from AVSI $i_{\mu x(abc)}$ respectively. The load currents are distorted and unbalanced. The MVSI

supplies balanced sinusoidal currents during grid supporting and injecting modes. The auxiliary inverter compensates the unbalanced components and harmonics in load currents, so the currents from AVSI are perfectly balanced and sinusoidal.

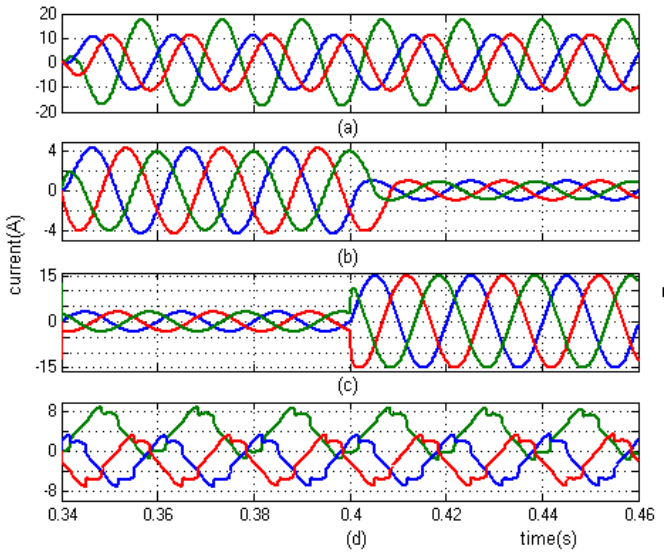

Fig.8. simulated performance of DVSI: (a) load currents; (b) grid currents; (c) MVSI currents; (d) AVSI currents

Fig.9(a) shows that the fundamental positive sequence of PCC voltages and grid currents are in phase during grid supporting mode and they are out of phase in grid injecting mode. Fig.9(b) shows that MVSI current is always in phase with fundamental positive sequence voltage. Thus the compensation capability of AVSI makes the source current and MVSI current at unity power factor operation.

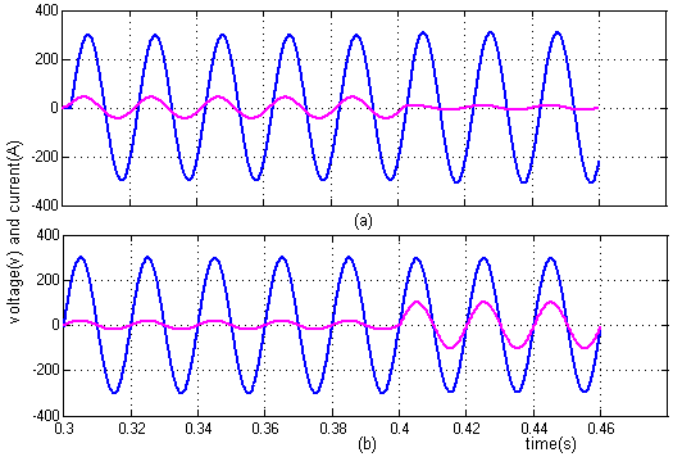

Fig.9. Grid sharing and grid injecting modes of operation; (a) PCC voltages and grid current in phase(a); (b) PCC voltage and MVSI current in phase(a)

The total harmonic distortion (THD) is a measurement of distortion of harmonics present in current and voltage. In power systems, THD value is used to study the power quality of the systems. The higher THD value means system has more harmonics and low power quality. The lower THD value means system has fewer harmonics and more power quality. From fig.10 the THD value of load currents using two-level inverter is 29.77%. This value can be reduced by increasing the levels of the inverter. As the inverter level increases, the harmonics present in the current are decreased. This can be achieved by using SPWM technique. In SPWM, the output of inverter is compared with pure sine wave and resultant output waveform shows reduction in harmonics. As the harmonics are reduced the THD value also decreases. This is shown in fig.11. Similarly FFT analysis of load voltages through of two-level and five-level inverter is shown in fig 12 and 13.

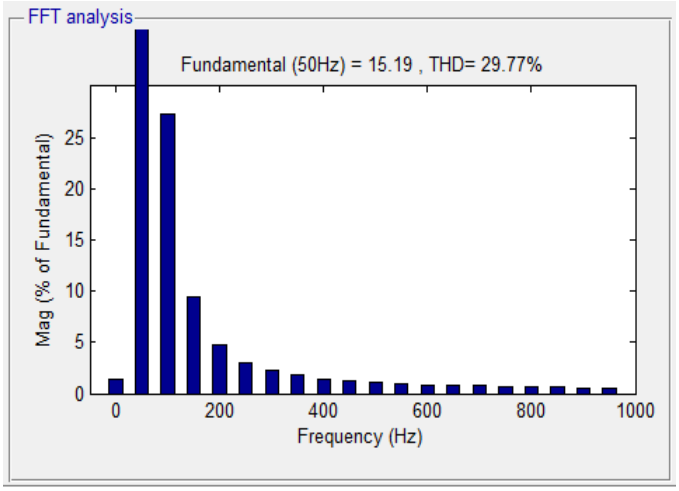

Fig.10. FFT analysis of load currents using two-level inverter

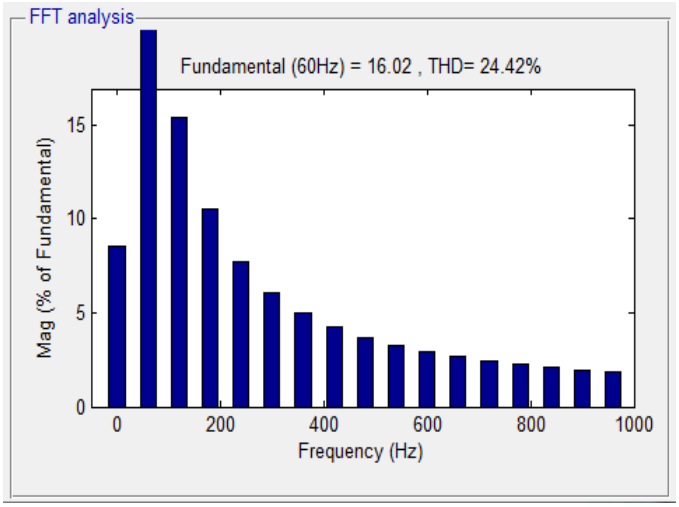

Fig.11. FFT analysis of load currents using five-level inverter

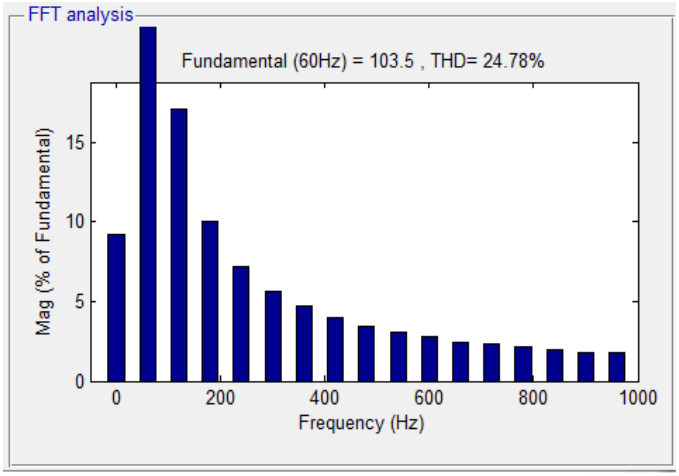

Fig.12. FFT analysis of load voltage using two-level inverter

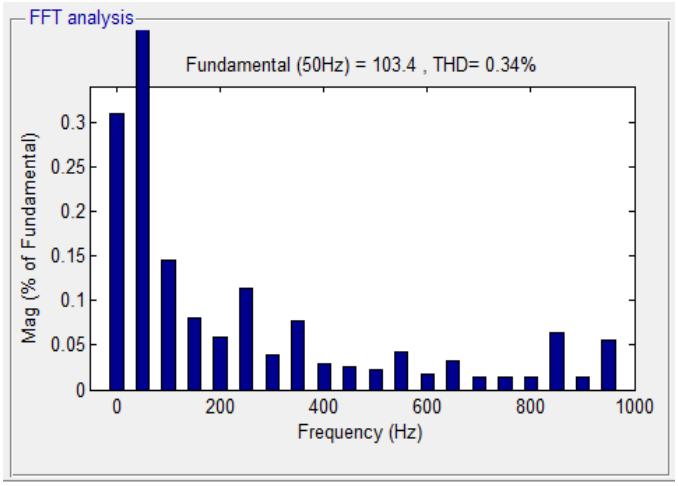

Fig.13. FFT analysis of load voltage using five-level inverter

5 CONCLUSION

The proposed DVSI scheme has the advantage to exchange power generated from the DER and also to compensate unbalanced and nonlinear load components. The control algorithm for the reference current generation is developed by using ISCT theory. As compared to a single level inverter, five-level inverter has less THD value for both load current and load voltage. By using sinusoidal pulse width modulation technique (SPWM), the output of the five-level inverter is more balanced and sinusoidal. Hence, there is no need of filter at the main inverter side. The DVSI method has advantages like increase in reliability, decrease in filter size and utilization of full capacity of five-level inverter to transfer real power from DER to load.

Table-1: Comparison of THD values

inverter	% THD value Load voltage (V_L)	% THD value Load current (I_L)
Two-level	24.78%	29.77%
Five-level	0.34%	24.42%

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