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Fast Optimization Method to Determine Setup and Hold Time for Analog IPs

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Abstract - *This work highlights the study a fast methodology to determinate setup/hold time for analog IPs. It presents a new method of optimization to determine the Setup/Hold pairing for analog circuits using a binary search range of the input variables. This new method developed by Cadence tools is applied particularly on the pulsed flip-flop D in order to obtain the best compromise between circuit's speed and the reliability. The solution proposed in this article is to use of the fast technique using the "Eldo commands" to determine Setup/hold time based on dichotomy method.*

Key Words: Dichotomy, Bisection, Optimization, Analog IPs.

1. INTRODUCTION

Dichotomy or Bisection is a method of optimization which employs a binary search method to find the value of an input variable (target value) associated with a "goal" value of an output variable. The input and output variables may be of various types (for example, voltage, current, delay time or gain) related by some transfer function.
In general, use a binary search to locate the output variable goal value within a search range of the input variable by iteratively halving that range to converge rapidly on the target value. At each iteration the "measured value" of the output variable is compared with the goal value. Bisection is employed in both the "pass/fail" method and the "bisection".

1.1 Definitions and Terminology

Setup time is defined as the minimum amount of time before the clock's active edge by which the data must be stable for it to be latched correctly. Any violation in this minimum required time causes incorrect data to be captured and is known as setup violation [2].

Hold time is defined as the minimum amount of time after the clock's active edge during which the data must be stable. Any violation in this required time causes incorrect data to be latched and is known as hold violation[2].

1.2 Setup and Hold Violations

When designers analyze a design, they check that each path meets the setup and hold specification for the design library that you specify.

Setup violations happen when data changes less than T_{Setup} before the rising edge of the clock. Hold violations are similar to setup violations but data changes less than T_{Hold} after the rising edge of the clock. There is a window around every rising clock edge that has a width of (T_{Setup} +T_{Hold}) where the data can not change. Changing the data inside this window will cause metastability inside of the flip-flop. Depending on which side of the clock edge the data changes, determines if the data path violates setup or hold time [2].

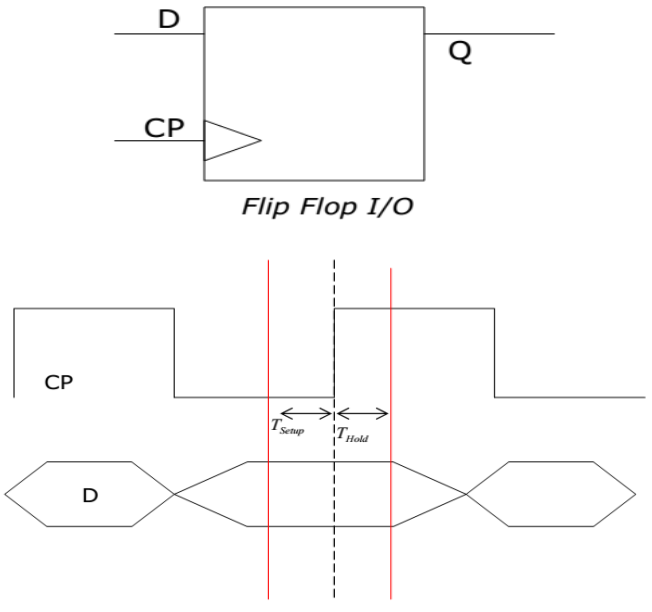

Fig -1: Setup/Hold Diagram

2. Bisection method

The bisection method is an algorithm used to search for the solution of a function. The method consists in repeatedly dividing the range of the input signal into two

parts and then selecting the sub-range in which the solution of the output signal is found.

The algorithm stops when the tolerance criteria for the output signal is reached.

To use bisection method, the following is required[5]:

- ✓ A user-specified pair of upper and lower boundary input variable values.

  For a solution to be found, one of these values must result in an output variable result > (goal value) and the other in a result < (goal value) : (for our case the goal is that V(Q)=0.5*VDD).
- ✓ Specified goal value(for our case: V(Q) changes thevalue from low to high or high to low level).
- ✓ Error tolerance value. The bisection process stops when the difference between successive tests values > error tolerance. Related variables.

  Variables must be related by a monotonic transfer function, where a steadily progressing time (increase or decrease) results in a single occurrence of the "goal" value at the "target" input variable value.

  The error tolerance is included in a relation used as a process termination criterion.

In the following part we will see how to use "Eldo commands" to determine Setup time and it's the same for the Hold:

"Eldo commands" fast methodology:

```
****measurements
.extract label= setup_time_Rise  xdown(v(CP),'0.5*V_VDD','0*per','10*per',2)' -
+ 'xup(v(D),'0.5*1.2','0*per','10*per',1)
**** DICHOTOMY METHOD
.OPTIMIZE METHOD=DICHOTOMY
.extract LABEL =Qval
+ max(V(Q),ts,tf)
+ Goal = '0.5*V_VDD'
.paramopt T10=('0.5*(tf+ts)',tf ,ts)
.tran .01n 12n
.probe tran   v(CP) v(D) V(Q)
```

With

```
.extract label= setup_time_Rise  xdown(v(CP),'0.5*V_VDD','0*per','10*per',2)' -
+ 'xup(v(D),'0.5*1.2','0*per','10*per',1)
```

Is a command to determine the setup value, see the T_{setup} in the **Fig -2 (**setup 01) in 2.1 section.

The optimization specification acting on unique analyses specified in the circuit netlist is achieved using the following command:
.OPTIMIZE + METHOD = PASSFAIL | DICHOTOMY|SECANT

For the bisection method:

.OPTIMIZE METHOD=DICHOTOMY

The following lines perform the transient analysis with Measure statement.
This statement measures the maximum voltage of output V(Q) in the interval between tf and ts. The analysis passes if the maximum output is greater than '0.5*V_VDD'. It fails if the maximum output is less than '0.5*V_VDD'.
The result (pass or fail) is stored in measurement name (Qval):

```
.extract LABEL =Qval
+ max(V(Q),ts,tf)
+ Goal = '0.5*V_VDD'
.paramopt T10=('0.5*(tf+ts)',tf ,ts)
```

2.1 Input Clock and Data Waveforms

To determine the setup and Hold values The Input Waveform D can be low to high (01) or high to low (10).

The following Figures show the four combinations.

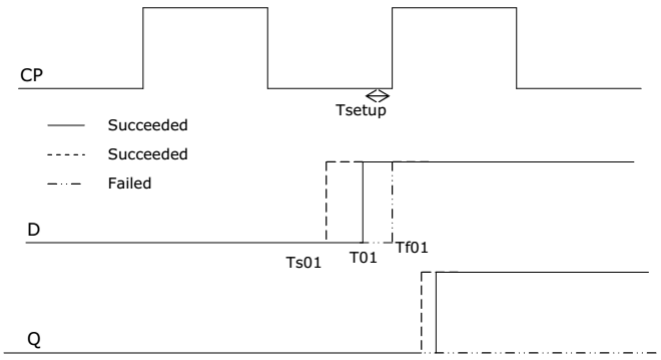

Fig -2: Setup 01

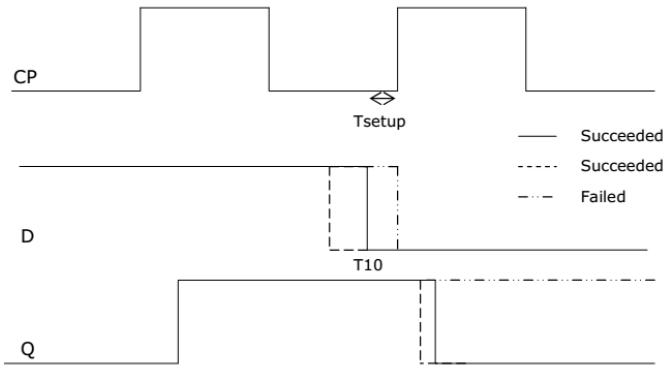

Fig -3: Setup 10

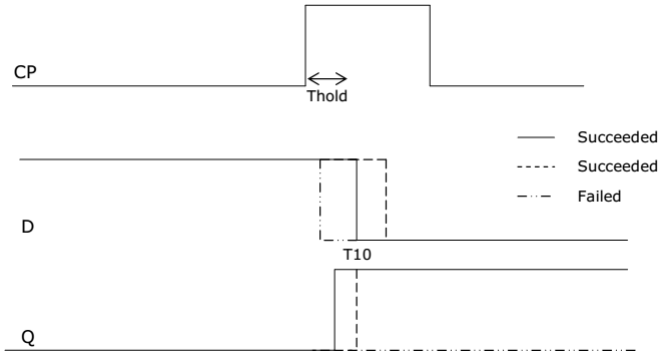

Fig -4: Hold 01

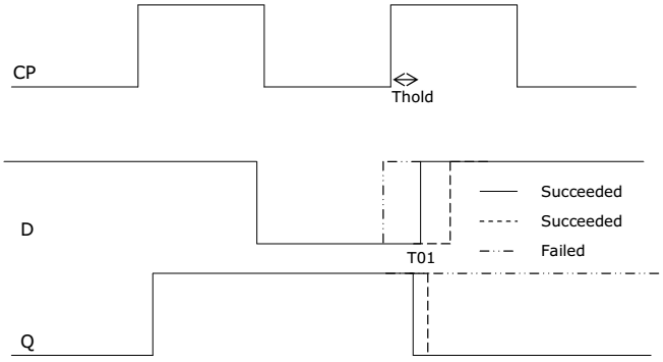

Fig -5: Hold 10

It can be clearly noticed that the proposed dichotomy technique globally offers good results.

3. CONCLUSIONS

This article shows the importance of the choice of the fast characterization methodology for the determinate Setup/Hold time for analog IPs. The solutions proposed by ELdo software [1] (kit for cadence company) provide the best compromise between circuit speed and reliability.

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BIOGRAPHY

Hamid BOUYGHF was born in Errachidia, in Morocco in 1982. He received the Engineer's degree in Microelectronics and telecommunications systems from FST- Fez in 2007. He is currently working towards the PhD degree in electronic engineering in Laboratory SSDIA ENSET Mohammedia. He interested in design and optimization of RF and Analog circuits. He is now a professor at Electrical Engineering Department in High School of Technology, Moulay Ismail University-Meknes-Morocco