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Design and Performance Analysis of Low Power Rail-to-Rail Op-Amp

Richa Yadav[1], Owais Ahmad Shah[2]

[1]Student, Dept. of VLSI Engineering, Noida International University, Greater Noida, U.P., India
[2]Asst. Professor, Dept. of Electronics and Communication Engineering, Noida International University, Greater Noida, U.P., India

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Abstract - *This paper presents the design and implementation of a 5-V compatible operational amplifier in a 3.3-V PDSOI technology, designed to operate from -180°C to 120°C. A low-power rail-to-rail operational amplifier (Op- amp) was realized in SMIC 0.18 µm CMOS process. Under a 1.8V supply voltage, a constant transconductance (within 5.4% of maximum variation) is ensured for the whole common-mode input range. The class AB output stage also has a full voltage swing. The circuit provides a gain bandwidth of 17.3-MHz and a DC gain of 99.6 dB. The input transistors operate in weak inversion, which have big g_m/I_d value, so the power consumption is reduced to only 89.02µW (C_{load}=5pf). The amplifier is comprised of a fully-differential input gain stage, single-ended output driver stage, and current reference for biasing. Wide temperature range operation is made possible with the use of a constant inversion coefficient current reference.*

Key Words: **Constant-g_m, CMOS analog integrated circuits, low power, Rail-to-Rail, Op-Amp, dB**

1. INTRODUCTION

Having the development of wireless communication from the second generation (2G) to 3G, many communication standards, such as GSM, TD-SCDMA, WCDMA and CDMA2000 will co-exist for a long time. This phenomenon will also happen in navigation and broadcast television, as there are also many standards, for example: GPS, Galileo, CMMB, DVB-H and so on. So, the reconfigurable radio frequency integrated circuit (RFIC) and broadband data conversion circuit facing multi-standard and multimode wireless communication is very important. For the key part of this circuit, i.e. the RF front-end transceiver, the often taken structure is the zero-intermediate frequency scheme, as there is no image-rejection problem, and consumes less power.

The operational amplifier (Op-amp) we proposed is suppose to be used between the down converter and the second stage ADC in the receiver end, and between DAC and the up-converter in the transmitting end. As the Op-amp has both input and output dynamic range rail-to-rail, we can lower requirement for ADC and DAC, thus to improve system performance. Also, battery powered device for communication such as cell phones drives IC to the low power. In this case, designing low-power Op-amp becomes the fundamental job of designing low-power analog and mixed signal systems. To reach the rail-to-rail amplitude, the input stage and the output stage should be designed respectively.

For the high supply voltage, there are some ways to make g_m constant. One of the often used ways is 1:3 current mirror method [8-11], in this way the g_m variation can be reduced to about 15%. Others are trans linear loops, Zener diodes, etc. And, the minimum supply voltage is usually about 2.5V. [12] For the low supply voltage, there are also some often used ways such as feedback loops [1], input level shift [2], bulk driving [3-4], current driven bulk[5], floating-gate MOSFET[6], DT MOS [7], 1:1 current mirror and so on. Our main goal is to realise a constant g_m input stage and a rail-to-rail output stage for a low-power operational amplifier. This has been achieved by the current-switch transconductance control circuit in the input stage and the improved class AB in the output one.

The paper is organized as follows. In section II, the input and the output part will be introduced and analyzed. In section III, the simulation results will be presented. Conclusion will be given in section IV.

2. THE PROPOSED METHOD

2.1 The input stage

By placing two complementary differential pairs in parallel as shown in Fig. 1, it is possible to obtain a rail-to-rail input stage. The nMOS pair is in conduction for high input common- mode voltages, in particular if

$$V_{SS} \geq V_{gsn} + V_{dsat} + V_{common} \quad (1)$$

While the pMOS pair is in conduction for low input common-mode voltages

$$V_{common} \geq V_{DD} - V_{dsat} - V_{sgp} \quad (2)$$

When both pairs are in parallel, the input dynamic range can be

$$V_{SS} < V_{common} < V_{DD} \quad (3)$$

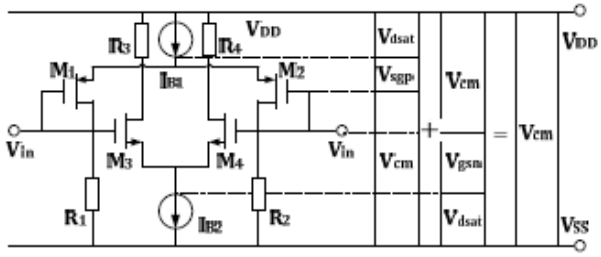

Fig- 1: Input range of complementary differential pairs

That is, rail-to-rail. To ensure this, the minimum supply voltage should be

$$V_{sup,min} = V_{sgp} + V_{gsn} + V_{dsatn} + V_{dsatp} \quad (4)$$

However, a main shortcoming of a rail-to-rail structure is that its total transconductance will change. That is, when the input voltage can make both pairs on, its total transconductance will be twice of that when only either pair is on. This will bring to the change of the loop gain and thus cause distortion. It will decrease phase margin and make the Op-amp unstable.

As the transistors in the proposed circuit work in weak inversion, their transconductance are proportional to the currents in them

$$g_{mi,weak} = \frac{I_p}{2n_pV_T} + \frac{I_n}{2n_nV_T} \quad (5)$$

Where, I_p and I_n are the current in the pMOS and nMOS pair, n_p and n_n are slope factors of the weak inversions. V_T is the thermal voltage.

So, to make g_m constant, we can tune the current within the input range, see Fig. 2.

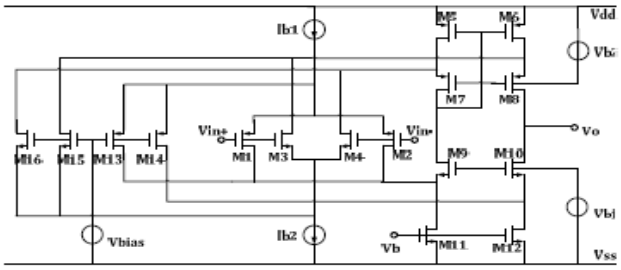

Fig- 2: Current switch transconductance control circuit

As can be seen from Equation (5) and Fig. 2, we set V_{bias} voltage to be 0.9 V. When the input voltage is low enough, pMOS differential pair M1 and M2 are on while nMOS differential pair M3 and M4 are off. Then, I_{b1} will come through M1 and M2, I_{b2} will come through M15 and M16, and so the total g_m will be

$$g_m = g_{mp} = \frac{I_p}{2n_pV_T} \quad (6)$$

When the input voltage is high enough, nMOS transistors M3 and M4 are on while pMOS transistors M1 and M2 are off. I_{b1} will pass through M13 and M14 while I_{b2} though M3 and M4, thus the total g_m will be

$$g_m = g_{mn} = \frac{I_n}{2n_nV_T} \quad (7)$$

When the input voltage is in the middle range, both pairs are on, the current switch M13, M14, M15, M16 will take away some of the current from I_{b1} and I_{b2}, thus the total g_m will be

$$g_m = g_{mn} + g_{mp} = \frac{I_p'}{2n_pV_T} + \frac{I_n'}{2n_nV_T} \quad (8)$$

Suppose the input voltage is 0.9 V, here M1~M4 will take 1/4 of the tail current, the expression will be

$$g_m = \frac{I_p}{4n_pV_T} + \frac{I_n}{4n_nV_T} \quad (9)$$

To have g_m constant, we should modify transistor size to make

$$\frac{I_p}{n_p} = \frac{I_n}{n_n} \quad (10)$$

Here the input stage delivers a constant output current to the summing circuit, which consist a high-swing current mirror (M5-M8) and common-gate stage (M9,M10). Gain can be improved by raising the tail current, however, to make sure input transistors are in weak inversion, the width and length of input transistors should be improved which at the same time can lower the offset of the circuit.

2.2 The Output Stage

In this work, output stage takes the improved feed-forward class AB circuit. For this circuit as shown in Fig. 3, M27 and M28 are the output part. M19 and M20 form a class AB control circuit. Points A and B have a small DC voltage, which can make sure that output transistors will not both be off thus to avoid cross-over distortion. From Fig. 3, we know

$$V_{gs19} + V_{gs27} = V_{gs22} + V_{gs23} \quad (11)$$

$$V_{gs20} + V_{gs28} = V_{gs25} + V_{gs26} \quad (12)$$

Let M19 and M22, M20 and M25 have the same size, then $V_{gs27} = V_{gs23}$, $V_{gs28} = V_{gs26}$. The quiescent current can thus be expressed as

$$I_q = \frac{(\frac{W}{L})_{27}}{(\frac{W}{L})_{23}} I_{21} \quad (13)$$

Here we suppose the currents in M21 and M24 are the same, and the following equation is satisfied

$$\frac{(\frac{W}{L})_{27}}{(\frac{W}{L})_{28}} = \frac{(\frac{W}{L})_{23}}{(\frac{W}{L})_{26}} = \frac{(\frac{W}{L})_{22}}{(\frac{W}{L})_{25}} = \frac{(\frac{W}{L})_{19}}{(\frac{W}{L})_{20}} \quad (14)$$

To make the quiescent current stable, M29 and M30 were added as floating current source, so as to bias the class AB control circuit. Here M29 and M30 has two parts to play, one is to compensate the effect of voltage source, as they

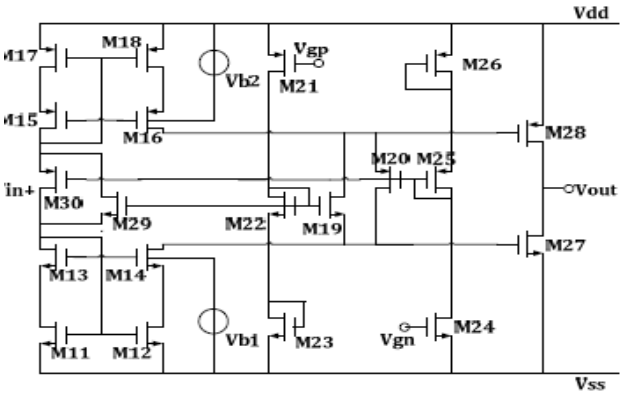

Fig-3: The improved output structure with floating current source

are the same structure of M19 and M20. In this way, PSRR of the circuit can be improved. The second is to make the quiescent current stable, less affected by the common mode input voltage. The whole circuit can be seen in Fig. 4. From Fig. 4, we see that the cascaded Miller frequency compensation method was used. Compared to the classical Miller compensation, this method shifts the non-dominant pole to higher frequency.

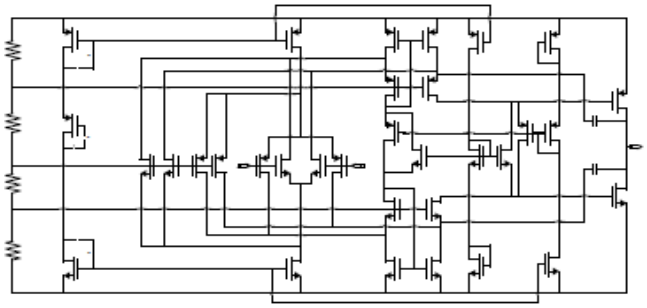

Fig-4: The proposed op-amp circuit

3 SIMULATION RESULTS

Based on the proposed circuit in Fig. 4, a rail-to-rail input/output Op-amp has been designed in SMIC 0.18-μm CMOS technology. The Op-amp is currently being fabricated in SMIC. So only the post-layout simulation results will be presented here.

Fig. 5 presents the simulated results of both the total and the individual g_m contribution of the input stage, versus $V_{i,cm}$ for V_{dd}=1.8V. The simulated g_m variation is 5.4%. Fig. 6 shows the frequency response of the Op-amp for different $V_{i,cm}$ values. The DC gain (A_{v0}), gain bandwidth product (GBW), and phase margin (PM) better than 99.2 dB, 16.6 MHz and 65.3° respectively has been achieved. Form Fig. 6 we can also see that the GBW and PM of this

Op-amp remain almost independent of $V_{i,cm.}$ Fig. 7 is the layout of the Op-amp.

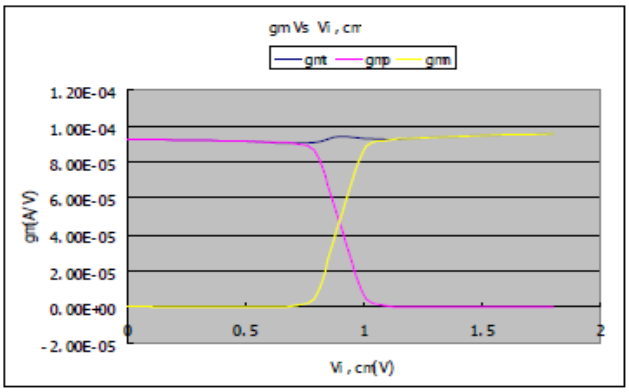

Fig-5: Simulated g_m verses $V_{i,cm}$ of the input stage

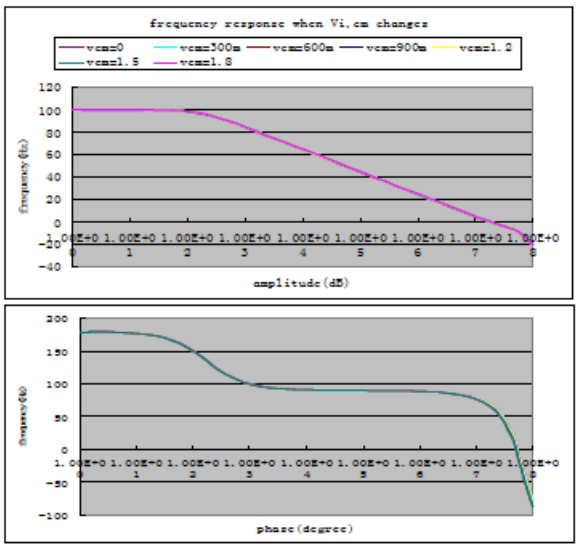

Fig-6: Frequency response of rail-to-rail amplifier

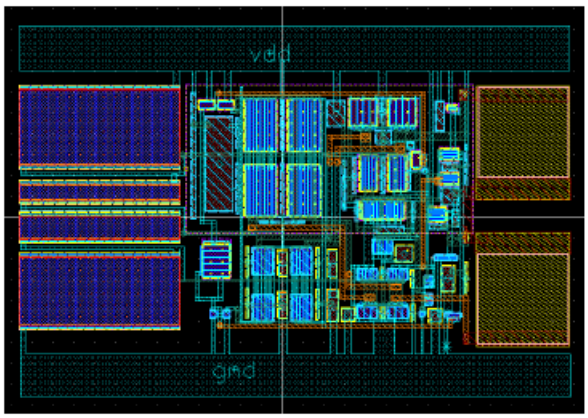

Fig-7: Layout of rail-to-rail amplifier

The simulated characteristic of the Op-amp with a 5-pF load at $V_{i,cm}$=0.9V are summarised in Table I.

Table- 1: Op-amp characteristics (post-layout) simulation with 1.8-V supply voltage, 5-pF load capacitance

DC gain (dB)	98.4
GBW (MHz)	17.3
Phase Margin (degree)	66.6
Power Consumption (μW)	89.01
Slew Rate + (V/μs)	10.61
Slew Rate - (V/μs)	10.46

CMRR @1 Hz (dB)	86.52
PSRR @1 Hz (dB)	9103
Input offset voltage @27°C (μV)	2.184
Input stage swing (0~1.8)	Rail-to-rail
Output stage swing (0~1.8)	Rail-to-rail
Chip Area (μm square)	135×65

According to Equation (4), suppose V_{dsat} is 0.1V, and the threshold voltage of transistors are 0.4V, the Op-amp given can still work when the supply voltage is 1.2 V. In this case, simulated results show that the gain of the circuit is 81.87 dB. Also, a GBW of 991.29 kHz is achieved.

4 CONCLUSIONS

In this paper, a constant-g_m rail-to-rail operational amplifier has been developed. The circuit can work after the down converter or before the up-converter in the RF transceiver in the zero intermediate schemes which are widely used in today's software defined radio for multi-standard and multimode wireless communication. The Op-amp consumes very little power which makes it appropriate for the battery powered devices like mobile phones, as the handheld terminal of wireless communication.

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