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An Efficient Design of 16- bit Parallel ADDER/SUBTRACTOR Using Reversible Gate

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Abstract - *In computation because of low power dissipation reversible logic is an attractive field of research in quantum and optical computation. In this brief we design a 16-bit adder/subtractor using 5*5 Parity Preserving Reversible Gate (P2RG).In this method we use the reversible logic gates in place of traditional logic gates like AND gate and OR gate. The function of P2RG adder is same as the traditional adder but the significant of the P2RG is that it works as adder as well as subtractor. The presented P2RG adder reduces the information bit use and loss by reusing the logic information bits logically and realizes the goal of lowering power consumption. It is also efficient in terms of gate count, constant inputs and garbage value.*

***Key Words*: Reversible logic; Parity Preserving; P2RG; Adder/Subtractor**

1. INTRODUCTION

To design an IC system, the power consumption is major concern. Reversible logic has a salient feature that can realize computation unit with almost zero power dissipation. However, there is a need to convert the reversible circuits into fault tolerant reversible circuits to detect the occurrence of error. Parity preserving is used for fault tolerance.

Landaure[1] proved that for irreversible computation, each bit of information loss generates KTln2 joules of heat energy, where K is Boltzmann's constant and T is the Absolute temperature at which computation is performed [1]. This is the minimum energy to process a bit. From the thermodynamics point of view it is also proved that KTln2 energy dissipation would not occur, if a computation is carried out in reversible way [2].

The idea behind the reversible computing is that electric charge on the storage cell consisting of transistor is not permitted to flow away when the transistor is switched [3]. Then it can be reused through reversible computing which can decrease the energy consumption. When there is no loss of information bit, then the system is reversible. Parity checking is one of the widely used error detection Method in digital logic and data communication systems. That's why most of the arithmetic functions is not parity preserving. If the parity of the input data is maintained throughout the computation, no intermediate checking would-be required [8]. A sufficient requirement for parity preservation of a reversible circuit is that each gate be parity preserving [8].Thus, we need parity preserving reversible logic gates to design parity preserving reversible circuits.

The rest of brief is organized as follows: background on reversible logic gates is given in section II. Some definitions related to reversible gate are given in section III. Idea behind P2RG is given in section VI. Proposed work is shown in section V. Results are shown in section VI. Finally conclusion and future work are made in section VII.

2. REVERSIBLE LOGIC GATES

Reversible computing is a model of computing where the computational process to some extent is reversible, i.e., time-invertible. A necessary condition for reversibility of a computational model is that the relation of the mapping states of transition functions to their successors should at all times be one-to-one. Reversible computing is generally considered an unconventional form of computing. To implement reversible computation, estimate its cost, and to judge its limits, it is formalized it in terms of gate-level

circuits. For example, the inverter (logic gate) (NOT) gate is reversible because it can be undone. The exclusive or (XOR) gate is irreversible because its inputs cannot be unambiguously reconstructed from an output value. However, a reversible version of the XOR gate—the controlled NOT gate (CNOT)—can be defined by preserving one of the inputs. More generally, reversible gates have the same number of inputs and outputs. A reversible circuit connects reversible gates without fan out and loops. Therefore, such circuits contain equal numbers of input and output wires, each going through an entire circuit.

Reversible logic circuits have been first motivated in the 1960s by theoretical considerations of zero-energy computation as well as practical improvement of bit-manipulation transforms in cryptography and computer graphics. Since the 1980s, reversible circuits have attracted interest as components of quantum algorithms, and more recently in photonic and nano-computing technologies where some switching devices offer no signal gain.

3. SOME DEFINATIONS RELATED TO REVERSIBLE GATE

Definition 3.1. Let the input vector be IVand output vector be OV, where IV = (I1, I2, ...,In), OV = (O1, O2, ..., On) and IV ↔ OV A n×n reversible gate is n-inputs and n-outputs circuit that produces a unique output pattern for each possible input pattern [9].

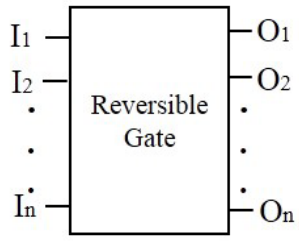

Fig -1: n×n reversible gate

Definition 3.2.The output that not used as a primary output or as input to other gate is called garbage output. These are only used to maintain the reversibility.

Definition 3.3. Number of gates that are used to realize the system is called gate cont [5].

Definition 3.4. The number of input that are to be maintained constant at either 0 or 1 in order to synthesize the given logic function is called constant inputs.

4. PARITY PRESERVING REVERSIBLE GATE

Parity preserving can be used as for the fault tolerance computation. Faults in the circuit can be detected by comparing the parity of inputs and outputs. The idea of the parity preserving property in the design reversible logic circuits was given by Parhami [8]. It is known that reversible gates have an equal number of inputs and outputs. Therefore, for parity preservation, this is sufficient to prove that parity of inputs and outputs should be equal. As an example, in parity preservation, 4*4 reversible gate must satisfy the equation which is given below:

$$A \oplus B \oplus C \oplus D = P \oplus Q \oplus R \oplus S$$

Where A, B, C and D are gate inputs and P, Q, R and S are gate outputs. Some Existing Fault Tolerance Reversible Gate are as follows:

Feynman Double Gate (F2G):

Fig. 2 shows 3*3 Feynman Double Gate (F2G) [5]. It has A, B and C input vector and output vector as P = A, Q = A⊕ B, and R = A⊕C.

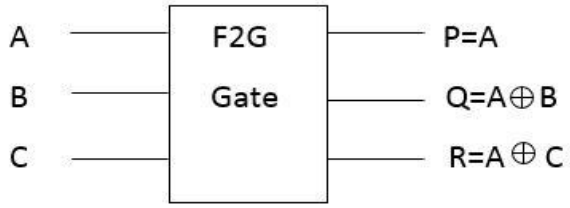

Fig -2: Feynman Double Gate (F2G)

Fredkin Gate (FRG):

Fig. 3 shows 3*3 Fredkin gate (FRG) [6]. It has A, B and C input vector and output vector as P = A, Q= A'B⊕ AC and R = A'C⊕ AB.

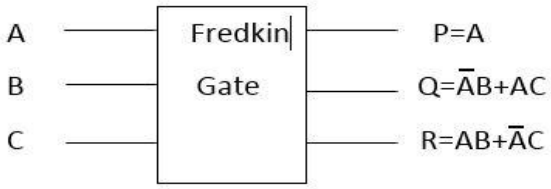

Fig -3: Fredkin Gate (FRG)

Modified IG Gate (MIG):

Fig. 4 shows 4*4 Modified IG [7] gate. It has A, B, C and D input vector and output vector as P = A, Q = A⊕ B, R = AB ⊕C and S = AB'⊕D.

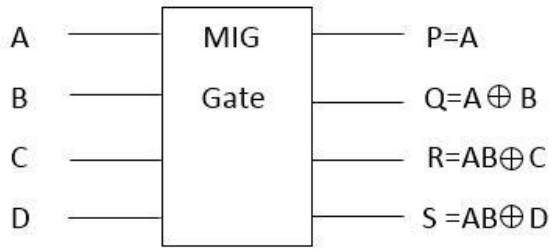

Fig -4: Modified IG Gate (MIG)

Parity Preserving Reversible Gate (P2RG): Fig.5 shows 5*5 parity preserving reversible gate [10], P2RG. It has A, B, C, D and E input vector and output vector as P=A, Q= (A'C'⊕B') ⊕D, R= (A'C'⊕B') D⊕AB⊕C, S=AB'⊕C⊕ (A'C'⊕B')'D and T= (D⊕E) ⊕AC.

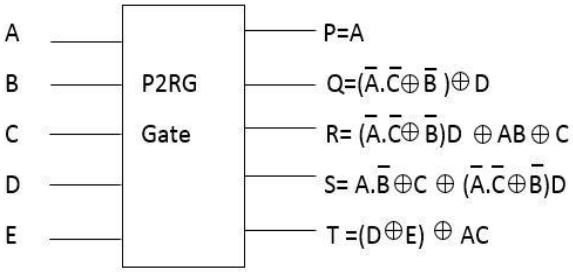

Fig -5: Parity Preserving Reversible Gate (P2RG)

5. PROPOSED WORK

The 16-bit 5*5 P2RG adder/subtractor can be realized by cascading two 8-bit 5*5 P2RG adder/ subtractor. The carry/ borrow from one first adder/subtractor will be propagate to the next adder/subtractor. A control line ctrl is used to control the mode of operation. If ctrl is set at logic '0' the circuit will perform addition and if it logic '1' it will perform subtraction. We are also comparing this work with the previous work in terms of garbage value, constant input and gate count.

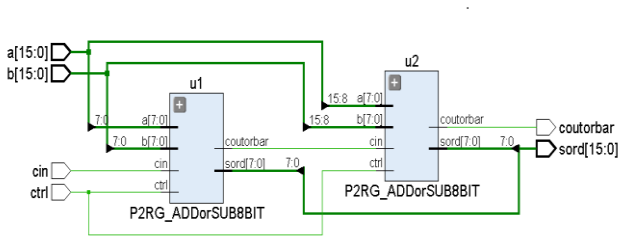

Fig.6 16-bit parity preserving parallel adder/subtractor.

6. RESULTS

The table shows the comparative results of different parity preserving reversible gate adder/subtractor. Table 1 comparative results of different fault tolerance adder/subtractor

Table -1: Adder/subtractor

GATE	Width	Gate count	Constant	Garbage output
F2G [9]	4	31	31	38
	8	67	67	82
	16	139	139	170
MIG [4]	4	17	17	24
	8	37	37	52
	16	77	77	108
5*5 P2RG	4	8	9	16
	8	16	17	32
	16	32	33	64

Table 2 and table 3 comparison of proposed work with existing work

Table -2: Adder/subtractor existing values

Gate	Gate count	Constant	Garbage output
F2G	139	139	170
P2RG	32	33	64
% reduction	76.97	76.26	62.35

Table -3: Adder/subtractor proposed values

Gate	Gate count	Constant input	Garbage output
MIG	77	77	108
P2RG	32	33	64
% reduction	58.44	57.14	40.74

7. CONCLUSIONS

The proposed circuit was compared with the existing designs in terms of constant input, garbage output and gate count. The design offers less gate count, less garbage output and constant input. The reversible computation done efficiently. In future we are planning to design more optimized parity preserving adder/subtractor design and other fault tolerance circuits i.e. less garbage output and constant input.

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