A REVIEW ON DESIGNING OF 4 BIT ALU USING GDI TECHNIQUE AT 45NM, 32NM, 22NM

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Abstract - *This paper demonstrates a design of a low voltage, low power, low area 4-bit arithmetic logic unit (ALU) by using the concept of gate diffusion input (GDI) technique. GDI(Gate diffusion input) a technique of low power digital combinational design. This technique allows less power consumption and reduced propagation delay for low-power design of ALU. In this number of transistor of GDI is reduced to half transistor as compared to CMOS transistor. Therefore Delay is less and power is reduced and speed is increased compared to CMOS. The main advantage of GDI is that it does not require vdd and gnd as a supply to a GDI cell. In this technique gate of PMOS and NMOS is diffused. The simulation shows that the design is more efficient with less power consumption, less surface area and is faster than CMOS techniques. The design and analysis is performed using 22 nm, 32 nm and 45 nm CMOS technology in Tanner EDA Tool. And also shows the difference between these technologies for power dissipation and number of transistor.*

Keywords: **GDI technique, ALU, Full Adder, CMOS, Low Power, Power dissipation, Area.**

1. INTRODUCTION

In VLSI, such as DSP and microprocessors, logic gates and arithmetic circuits are very much used. In that most commonly used operations of these circuits are AND, OR, addition, subtraction and multiplication. In arithmetic circuits, the building block of all digital circuits are Logic gates also full adder cell is the extensively used in it. Recently in mobile communication and computation, building low-power systems has emerged as highly in demand because of the fast growing technology. As these is the era of growing technology and scaling of devices up to nanometer regime, the Arithmetic and Logic circuits are to be designed with less power, compact size and propagation delay. In any digital system a processor is an important part. An ALU is one of the main components of a microprocessor. Basically ALU is a combinational circuit that performs arithmetic and logical operations on a pair of n bit operands. The arithmetic logic circuits are to be designed with compact size, less power and propagation delay. CMOS uses both PMOS and NMOS transistors. CMOS design gives high power dissipation, and high delay. Cell can be design with less power consumption, less area and can be faster as compared to CMOS techniques by using GDI technique cell.

In GDI cell using only two transistors allows implementation of a wide range of complex logic functions.GDI method is suitable for design of fast, low power circuits, using reduced number of transistors as compared to CMOS, while improving power characteristics and allowing simple Shannon's theorem-based design by using small cell library. The aim of this work is to examine a typically in order to explain and interpret the GDI technique and compared with CMOS technique. This paper demonstrates the concept of GDI technique for design of ALU. In this paper ALU is designed by using GDI technique.

Vaijayanti Panse et.al [1] He proposed the work "Minimization of Transistors Count for 2:1 MUX using GDI Technique" .GDI technique is used to reduce the number of transistors compared to conventional CMOS design. The designs are implemented using 90nm cmos process in Microwind3.1v and DSCH3 and their respective simulation results. Biswarup Mukherjee et.al [2] He proposed work "Design & Study of a Low Power High Speed Full Adder Using GDI Multiplexer". He proposed a new method for implementing a low power full adder by means of a set of Gate Diffusion Input (GDI) cell based multiplexers. Simulated outcome using state- of-art simulation tool shows finer behavioral performance of the projected method over general CMOS based full adder. Here conventional FA & proposed 12-T full adder circuits are analyzed in standard simulator using 250 nm technologies. Amanpreet Kaur, [3] he proposed work "Comparative Analysis of GDI based D Flip Flop Circuits using 90nm and 180nm Technology ". He proposed D flip flop design topologies has been developed and analyzed.

The evaluation is carried out by tanner tool with 180 nm & 90 nm technology. Performance comparison is presented with respect to number of transistors, power dissipation and delay. Arkadiy Morgenshtein[4] He proposed work "GDI (Gate Diffusion Input) - a new technique of low power digital circuit design. He proposed this technique allows reducing power consumption, delay and area of digital circuits, while maintaining low complexity of logic design. A prototype test chip of 8-bit CLA Adder has been fabricated, based on GDI and CMOS cell libraries, showing up to 45% reduction in power-delay product in GDI. These are the previous work done. In this paper 4 bit ALU is implemented in tanner at 22nm, at 32nm and at 45 nm. Number of transistor is reduced and therefore Area is reduced.

1.1Gate Diffusion Input technique

Main concept of GDI is that gate of PMOS and NMOS is diffused. In these days in digital circuits design, for a digital circuit designer's a high speed, high throughput and small silicon area and also low- power consumption in digital circuit is most essential things for a designers. GDI is such a technique that we can use for design of low power digital circuits. And it is also a novel design method of a low power digital circuit. In GDI cell using only two transistors allows implementation of a wide range of complex logic functions. In GDI by using only two transistor (PMOS AND NMOS) many function such as AND, OR, XOR and XNOR can be implemented.GDI method is suitable for designing of fast, low power circuits, using reduced number of transistor as compared to CMOS techniques and also improving power characteristics. As compared to CMOS, fast, low power circuits can be designed bu using gdi technique. The main advantage of GDI is that it require less number of transistors as compared to CMOS. Therefore area is reduced. Therefore delay is less and speed is increased. Morgenshtein has proposed basic GDI cell shown in Fig.1. A new approach for designing low power digital combinational circuit is a GDI Technique. GDI technique is basically two transistor implementation of complex logic functions which provides in-cell swing restoration under certain operating condition. This approach leads to reduction in power consumption, propagation delay and area of digital circuits. while having low complexity of logic design. An important feature of GDI cell is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. Drain terminals of the two transistors are taken as output. Source terminal of Pmos is acting as one input, and Source of Nmos is acting as another input. Therefore GDI cell gives two extra input pins for use which makes the GDI design more flexible than CMOS design.

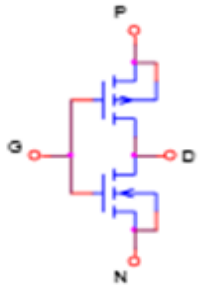


Fig.1.1 Basic GDI Cell

There are three inputs in a GDI cell - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).Bulks of both NMOS and PMOS are connected to N and P respectively. Table 1.1 shows different logic functions implemented by GDI logic based on different input values. So, various logic functions can be implemented with less power and high speed with GDI technique as compared to conventional CMOS design.

BASIC FUNCTIONS USING GDI CELL

N	P	G	OUTPUT	FUNCTION
0	1	A	A'	INVERTER
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
B'	B	A	A'B+B'A	XOR
B	B'	A	AB+A'B'	XNOR

Table 1.1

It can be seen that large number of functions can be implemented using the basic GDI cell. MUX design is the most complex design which requires 8-12 transistors with the traditional CMOS, that can be implemented with GDI, which requires only 2 transistors. Many functions can be implemented efficiently by GDI with minimum number of transistor. Function1 and Function2 are universal set for GDI, and consists of only two transistors, compared to NAND and NOR. When compared to CMOS, the GDI Technique use less transistors and power dissipation is also less. A new technique of low power digital circuit design is a GDI (Gate Diffusion Input). Power consumption, delay and area of digital circuits is reduced by This technique, maintains low complexity of logic design. Since GDI cell has no power supply connected to it, there will be a voltage drop at the output. This drop will be negligible for small circuits. Implementations of GDI circuits in SOI or twin-well CMOS processes are expected to supply more power- delay efficient design,

due to the use of a complete cell library with reduced transistor count. Because of less number of transistors, the switching is reduced and hence there will be a less power, delay and also reduced area. Because of the less number of transistors the switching node capacitance will be reduced that results in reduction of dynamic power

1.2 ALU

An ALU is one of the main components of a microprocessor.ALU also contribute to one of the highest power- density locations on the processor, as it is clocked at the highest speed and is busy mostly all the time which results in thermal hotspots and sharp temperature gradients within the execution core. Therefore, this motivate us strongly for a energy-efficient ALU designs that satisfy the high- performance requirements, while reducing peak and average power dissipation. Basically ALU is a combinational circuit that performs arithmetic and logical operations on a pair of n bit operands. Arithmetic Unit Employing fast and efficient adders in arithmetic logic unit will aid in the design of low power high performance system. In this paper Arithmetic Unit consists of adder and substractor and logical unit consists of AND, OR.

2. DESIGNING OF ALU USING GDI TECHNIQUE

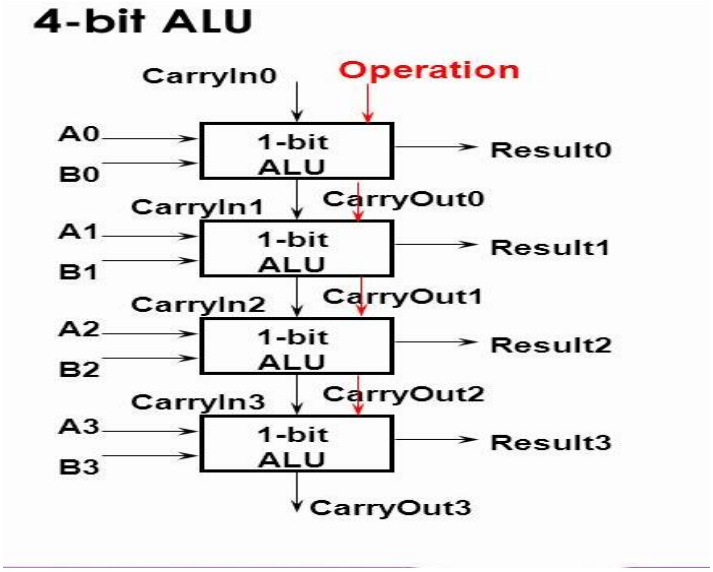


Fig 2.1: 4 bit ALU

ALU can perform various logic operations like NOT, AND, OR, NAND, NOR, XOR, XNOR etc. For these operations a special unit is made called as Logical Unit. This Logic Unit performs all logic operations asked to perform. A MUX operated by select lines, for which particular logic operation to perform, is used inside this logic block.

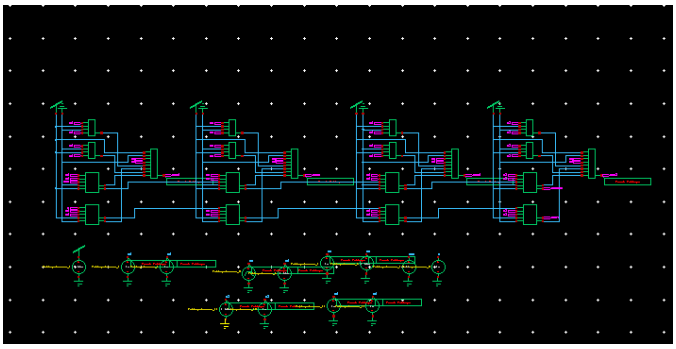


Fig2.2 4 Bit ALU using GDI technique

3 SIMULATON

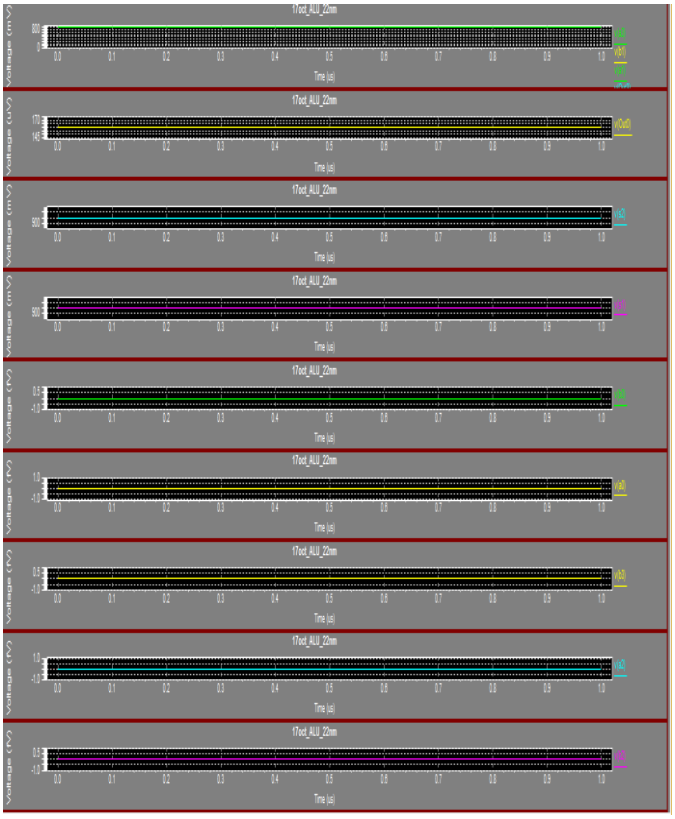


Fig 3: Waveform of 4 bit ALU

4 RESULT

1] Area

Technique	Area
CMOS	776
GDI	312

2] Power and Delay

	technique	45nm	32nm	22nm
Power	Simple	$4.22e^{-4}$	$5.11e^{-4}$	$6.53e^{-4}$
	GDI	$2.77e^{-5}$	$1.87e^{-5}$	$1.70e^{-5}$
Delay	Simple	$5.76e^{-8}$	$5.33e^{-8}$	$5.10e^{-8}$
	GDI	$2.80e^{-9}$	$2.51e^{-9}$	$2.22e^{-9}$

3] Comparison graph of power between CMOS and GDI

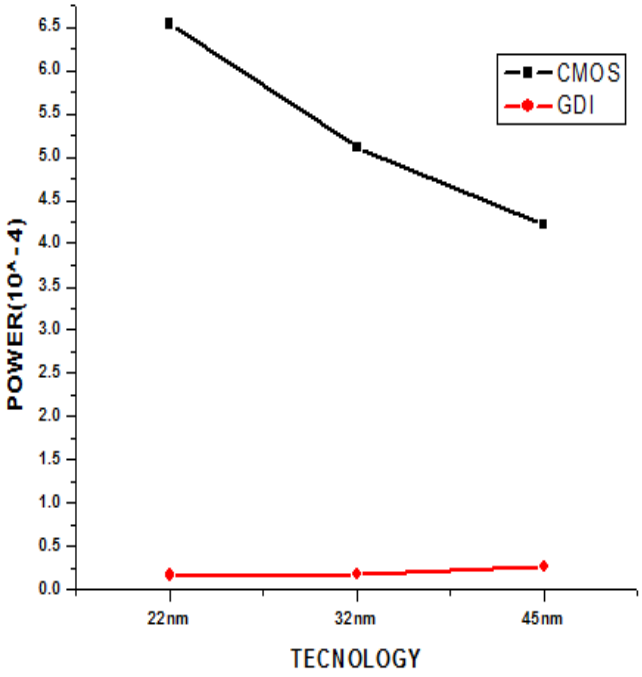


Chart -1: Power of GDI and CMOS

4] Comparison between CMOS AND GDI areas

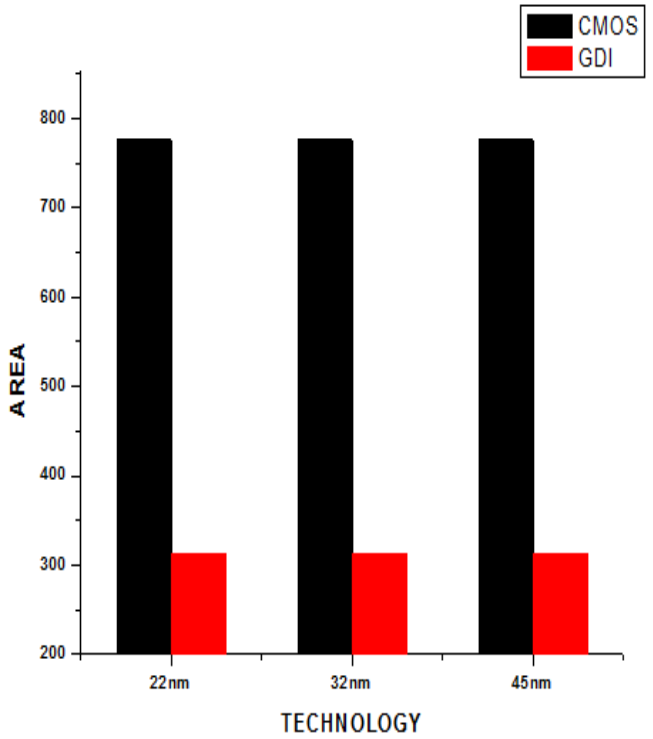
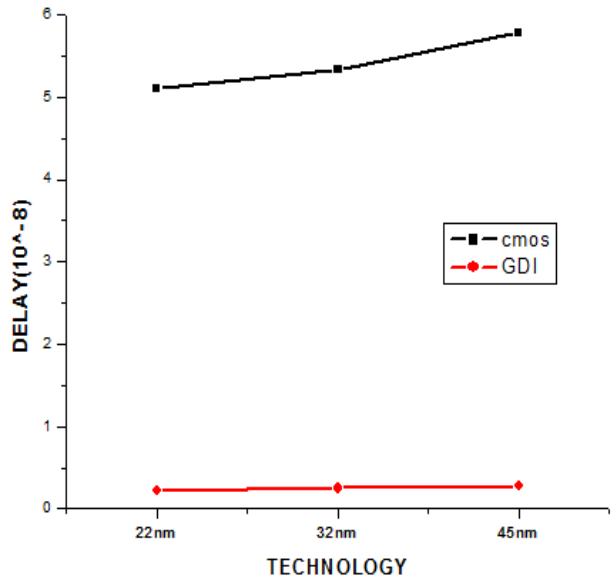


Chart -1: Area of GDI and CMOS

5] Comparison between CMOS AND GDI DELAYS



3. CONCLUSIONS

Power consumption in CMOS circuit is classified in two categorize: static power dissipation and dynamic power dissipation. In today's CMOS circuits static power dissipation is negligible thus not considered as compared to dynamic power dissipation. Dynamic Power dissipation in a CMOS circuit is given by P = CLf VDD2. The power supply is directly

related to dynamic power. The numbers of power supply to ground connections are reduced in GDI implementation which reduces the dynamic power consumption. In this paper we presented a novel low power and low transistor count 4 bit ALU and compared its performance for power consumption, area and delay. Analysis and simulation studies were performed on 4bit alu using GDI Technique. Power dissipation, propagation delay and the number of transistors of ALU were compared using CMOS, GDI techniques. GDI technique proved to have best result in terms of performance characteristics among all the design techniques. This work presents a 4-bit ALU designed in 250nm technology for low power and minimum area with GDI technique. The GDI technique has been proven to be superior to the CMOS in power dissipation, area and in propagation delay. The combination of low power and low transistor count makes the 4 Bit ALU Using GDI techniques a viable option for low power design. In this number of transistor of GDI is reduced to half transistor as compared to CMOS transistor. Therefore Delay is less and power is reduced and speed is increased compared to CMOS.

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