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FPGA Implementation of Pipelined CORDIC Processor for Trigonometric Function

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Abstract - *At present, several of the computations in signal process and wireless communication are connected with advanced analysis of many functions. These advanced functions are combination of circular function and trigonometric function terms that usually unfold within the channel. Most of those functions may be split into elementary functions. During this paper we have a tendency to present a hardware economical design by exploitation CORDIC algorithmic rule for the calculation of circular function and trigonometric functions. This approach is simulated exploitation Model Sim simulation package, synthesized exploitation Xilinx ISE style suite and therefore the planned design is enforced on Xilinx FPGA target device i.e. SPARTAN 6.*

Key Words: **Xilinx, FPGA SPARTAN-6, LUT (look up table), Arithmetic circuit, CORDIC, DSP**…

1. INTRODUCTION

The solutions for the planning of high speed VLSI architectures for time period digital signal process (DSP) algorithms are mapped from formula into hardware economical architectures. With the arrival of low value, low power FPGA's; style of such architectures which might satisfy the performance needs for the signal process applications like 3 dimensional (3D) graphics, video/image/ signal process systems has become easy. Many of the DSP algorithms uses the calculation of elementary functions like trigonometric, inverse trigonometric, logarithm, exponential, multiplication, and division functions that need high process power. The usually used package solutions for the digital implementation of those functions are table search methodology and polynomial expansions, requiring variety of multiplication and additions/subtractions. In 1959, Volder [6] has projected a special purpose digital computing unit referred to as COordinate Rotation data processor (CORDIC). This formula was at first developed for pure mathematics functions, exploitation givens rotation remodel technique. The CORDIC formula computes second rotation exploitation unvaried equations using shift and add operations that have easy design and consume less power. Walther has projected a unified formula to reckon rotation in circular, linear, and hyperbolic coordinate systems. The CORDIC formula performs numerous elementary functions attainable in rotation and vectoring mode of circular, linear, and hyperbolic coordinate systems [3][4]. CORDIC technique has been utilized in several applications, like signal process transformations, digital filters and matrix primarily based computations. Radical low power systems may be with efficiency developed by CORDIC [5] [6]. Additional recently, the advances within the VLSI technology and also the advent of EDA tools have extended the appliance of CORDIC formula to the sphere of medicine signal process, neural networks, package outlined radio, and MIMO systems etc.

1.1 PROBLEM DEFINATION

The primary objective of this project is to implement CORDIC processor adopting low power pipelined schemes with each parallel and pipelined on FPGA in VHDL, verify and check for its practicality and analyze its performance. There is a true would like of hardware economical algorithms within the present generation of technologies due to the extraordinary signal process demand required by them. Thus, the present trend is back toward hardware economical algorithms. Among

all those shift-and-add architectures normally called CORDIC have wide selection of engaging options which will reckon the majority elementary functions with straightforward architectures and any study on such rule may provide additional fascinating result which might be best suited to all this world application. Several of these applications need elementary calculations like sin and cos. Hence, we have a tendency to be presenting pure mathematics, index, hyperbolic and square rooting exploitation CORDIC rule and its performance report. The pipelined design takes the angle or section as input and offers each circular function and cos for the given input in preset variety of small rotations. These small rotations are set by accuracy demanded by the applying.

Section 1 figures out the review research done related to this topic. Primarily, the main motivation for current trend of switching on to CORDIC processors is discussed. Various issues contributing to this development is elaborated with enough citations. Section 2 briefly discusses the CORDIC algorithm, its operating modes and how the algorithm can be used for evaluating trigonometric functions. Section 3 presents the design of key modules for realization of the project and discusses the unrolled CORDIC architectures. The stepwise description of paper implementation stages are discussed here. Section 4 and 5 discusses the simulation results, details the application program mapped to design and finally, exemplifies the hardware FPGA realization on Spartan 6 device. Lastly, some of the possible research ideas and future directions are listed that will help to explore this paper further.

2. CORDIC ALGORITHM

The CORDIC is extremely easy and repetitive convergence formula that reduces complicated multiplication, greatly simplifying overall hardware quality. This is an attractive choice to system designers as they still face the challenges of reconciliation aggressive value and power targets with the accumulated performance needed in next generation signal process solutions. The essential principle underlying the CORDIC-based computation, and present its repetitive formula for various operational modes.

CORDIC formula has two sorts of computing modes Vector rotation and vector translation. The CORDIC formula was at first designed to perform a vector rotation, wherever the vector V with elements (X,Y) is rotated through the angle θ yielding a new vector V' with part (X',Y') shown in Fig.1.

$$V' = [R]\,[V] \qquad (1)$$

Where **R** is the rotation matrix

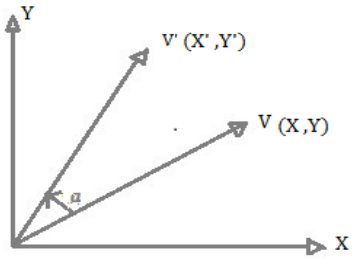

Fig -1: Vector Rotation

$$R = \begin{bmatrix} \cos\alpha & -\sin\alpha \\ \sin\alpha & \cos\alpha \end{bmatrix} \qquad (2)$$

$$R = \begin{bmatrix} \frac{1}{\sqrt{1+\tan\alpha^2}} & -\frac{\tan\alpha}{\sqrt{1+\tan\alpha^2}} \\ -\frac{\tan\alpha}{\sqrt{1+\tan\alpha^2}} & \frac{1}{\sqrt{1+\tan\alpha^2}} \end{bmatrix} \qquad (3)$$

By factoring out the cosine term in (3), the rotation matrix **R** can be rewritten as

$$R = \left[1 + \tan^2\alpha^{-\frac{1}{2}}\right] \begin{bmatrix} 1 & -\tan\alpha \\ \tan\alpha & 1 \end{bmatrix} \qquad (4)$$

And can be interpreted as a product of a scale-factor $K = [1 + \tan^2\alpha^{-\frac{1}{2}}]$ with a pseudo rotation matrix, given by Rc

$$Rc = \begin{bmatrix} 1 & -\tan\alpha \\ \tan\alpha & 1 \end{bmatrix}$$

$$Rc = \begin{bmatrix} 1 & -\tan\alpha \\ \tan\alpha & 1 \end{bmatrix}$$

In vector translation, rotates the vector V with component (X, Y) around the circle until the Y component equals zero as illustrated in Figure 2. The outputs from vector translation are the magnitude X' and phase θ', of the input vector V.

After vector translation, output equations are:

$$X' = Ki = \sqrt{x^2 + y^2}$$

$$Y' = 0$$

$$\theta' = atan(\frac{y}{x})$$

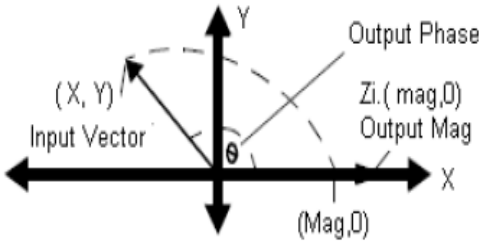

Fig -2: Vector Translation

To achieve simplicity of hardware realization of the rotation, the key ideas utilized in CORDIC arithmetic are to decompose the rotations into a sequence of elementary rotations through predefined angles that would be implemented with minimum hardware value and to avoid scaling, which may involve mathematical operation, like square-root and division. The second plan is predicated on the actual fact the scale-factor contains solely the magnitude data however no data regarding the angle of rotation.

After few years, Walther found however CORDIC iterations might be changed to calculate hyperbolic functions and reformulated the CORDIC rule in to a generalized and unified type that is appropriate to perform rotations in circular, hyperbolic and linear coordinate systems. The unified formulation includes a replacement variable n that is allotted completely different values for various coordinate systems. It is potential to capture the vectoring and rotation modes of the CORDIC rule altogether 3 coordinate systems employing a single set of unified equations. The generalized CORDIC is developed as follows:

$$x_{i+1} = \{x_i - ny_i\sigma_i 2^{-1}\}$$

$$y_{i+1} = \{y_i + nx_i\sigma_i 2^{-1}\}$$

$$z_{i+1} = \{z_i - \tan^{-1} 2^{-i}\}$$

Here $\sigma i = \{sign(zi)$ for rotation mode , $-sign(zi)$ for vectoring mode.}

3. CORDIC ARCHITECTURE

CORDIC algorithmic program is enforced in a very range of the way. A direct mapping of equations four, five and six in hardware results in associate degree iterative design. The iterative architectures is also either word-serial or bit-serial, relying on whether or not the functional unit implements the logic for one bit or for one word. The iterative design has to perform iterations at n times the information rate. The iterative structure is unrolled thus that every of the n process components continuously perform the same iteration. Unfolded architectures have two blessings initial the shifters is designed for fastened shifts, which means that they will be enforced within the wiring[1]. Second, the ROM that holds the constant values for the z-branch need not to be updated when each iteration. These constants will be hardwired instead of requiring storage area. The entire CORDIC processor is therefore reduced to associate degree array of interconnected adder- subtraction units as shown in figure one. The unfolded design is simply pipelined by inserting pipeline registers between the adder-subtraction units Figure 3 Unrolled CORDIC structure.

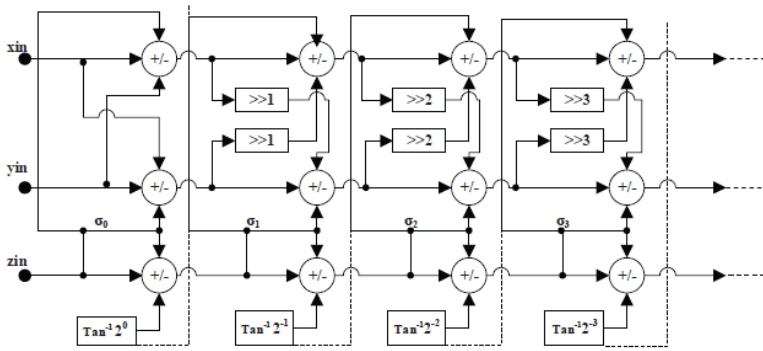

Fig -1: Unfolded CORDIC structure

4. SIMULATION RESULTS

The implementation in this work is targeted FPGA families viz. Spartan-6 .The implementation is carried out for associate input quantity length varying from 16 bits. The style synthesis, mapping, translation and simulation are applied in Xilinx ISE 14.5. The trigonometric function uses simple pipelined architecture using CORDIC processor. The CORDIC is operated in rotating mode, hence only angle is given as input and x, y values are given in the program .As this architecture inputs can be given at every clock pulse and the value for inputs will output after eight clock cycle as it.

As it is observed, that CORDIC processors are going to expand their existence in the future high performance. This leads to lower scalability. Since the algorithm involves only add and shift operations, it has very good hardware efficiency and a very minimal control overhead. The realization of this paper will solve most of the difficulties discussed above and in the problem definition section. This paper will have following results:

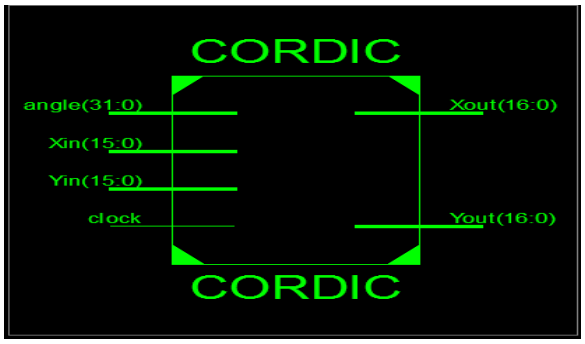

Fig -1: RTL Schematic of CORDIC Processor

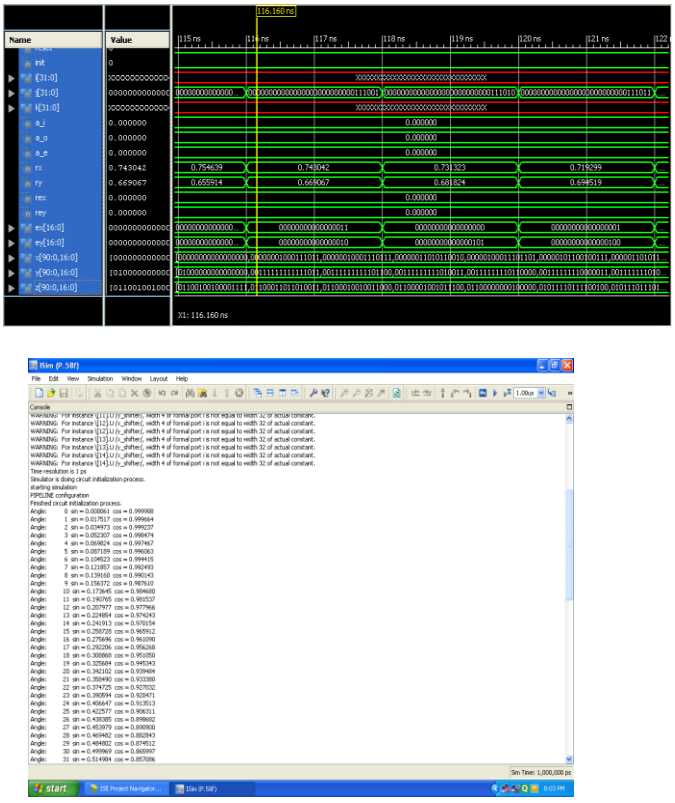

Fig -1: RTL Schematic and console of sine – cosine waveform CORDIC Processor

ADVANTAGES

CORDIC uses the same shift-add operation for all application. The first approach mainly achieved by reducing the complexity of barrel shifter and also by reducing the scaling factor. And reduced latency realization can be achieved by schemes like angle recording. Thus, these method will employ the advantages of methods leading to faster responsive system which is the current need of real time application specific ICs.

5. CONCLUSIONS

In this paper we have a tendency to present a hardware economical design by exploitation CORDIC algorithmic rule for the calculation of circular function and trigonometric functions. This approach is simulated exploitation Model Sim simulation package, synthesized exploitation Xilinx ISE style suite and therefore the planned design is enforced on Xilinx FPGA target device i.e. SPARTAN 6. CORDIC evaluates the rotational function more efficiently than MAC unit and also saves more hardware cost. Finally, the device utilization outline and temporal order reports are given and application are including image processing , communication system , motion prediction for robotics, control system for space comes under DSP domain.

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