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ULTRA LOW POWER, LOW VOLTAGE 16 BIT BCD ADDER USING DTMOS TECHNIQUE

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Abstract - *This paper demonstrates the design of low voltage, low power 16 bit BCD adder using DTMOS technique for low-power, low leakage current applications. The design goal is to achieve low leakage current and minimum power dissipation at lower supply voltage. DTMOS transistor is proposed in this paper for the design of BCD adder which replaces the normal CMOS transistors for designing a low power, low voltage, minimize leakage current 16 bit BCD adder. The design and analysis is performed using 22 nm, 32 nm and 45 nm CMOS technology in Tanner EDA Tool. And also shows the difference between these technologies for power dissipation and minimize leakage current.*

***Key Words*: Low power applications, 16 bit BCD adder, full adder, DTMOS, Low power, Low voltage.**

1. INTRODUCTION

From the past few years due to the extensive growth of market for portable devices such as cell phones, portable computers, other low power applications and also the design of analog circuits which requires low power, low voltage with high performance has become an important issue now a day's. One of the limitations for implementation of portable devices and design of other low power circuits at low voltage is the threshold voltage (Vth). For this reason reduction of threshold voltage is necessary for low-power, low-voltage operation. DTMOS technique is the best solution for reduction of threshold voltage (Vth).

Bhanu Kumar G, Vasudev Reddy T et.al [1] He proposed "DESIGN OF LOW VOLTAGE LOW POWER OPAM dtcmos". The proposed op-amp has been simulated in Cadence Virtuoso 180 nm CMOS technology under 5 pF load. The proposed opamp is designed for the purpose of low power applications. Ishan Varun, Tarun Kumar Gupta et.al [2] He proposed "Ultra-Low Power NAND Based Multiplexer and Flip-Flop". He had implemented 2 low power digital circuits 4*1 electronic device and JK master-slave flip-flop designed with NAND gates. These NAND gates are designed with combination of sleepy-eyed stack technique with reverse body bias (RBB) and twin threshold CMOS (DTCMOS).The Simulation results will be done in Tanner T-Spice at 65 nm. Selahattin Sayil, and Nareshkumar B. Patel et.al [3] He proposed "Soft Error and Soft Delay Mitigation Using Dynamic Threshold Technique". He had implemented an analysis on various DTMOS schemes for their soft error tolerance and have found that the standard DTMOS configuration increases circuit robustness due to increased current drive. This approach results in considerable area savings compared to driver sizing alone. He had considered 65nm technology with parameters obtained using the Predictive Technology Model. Naresh Kumar, Umesh Dutta and Dileep Kumar et.al [4] "An Analytical model of the Bulk-DTMOS transistor" He proposed a novel D flip-flop for low voltage operation with improved speed using SPICE simulation done using 180nm technology. It takes advantage of a dynamic threshold voltage using DTMOS for ultra-low voltage operation and a negative differential resistance storage using Bistable Gated Bipolar Device (BGB). DTMOS provides low power consumption and BGB provides high speed because of less capacitance.

CMOS circuits have scaled downward aggressively in each technology generation to achieve higher integration density and performance. With the current nanoscale technology trends in CMOS circuits, effective solutions have to be sought to reduce leakage power which is expected to dominate the chip's total power consumption in the near future. These solutions must be sought in all design abstraction levels: system and architectural level, circuit level, and process/device level. Body biasing technique is a circuit level approach to reduce leakage in scaled CMOS circuits. Dynamic threshold MOSFET (DTMOS) transistor utilizes dynamic body bias because in DTMOS, substrate (or body) and gate of MOSFET are tied together, therefore input gate voltage forward biases the source substrate junction and owing to the body effect threshold voltage (Vth) decreases in the ON state and when the gate is turned off, Vth returns to its original high value in equilibrium. DTMOS has proven to be an excellent alternative for the implementation of ultra-low power and high-performance circuits. This technique is popular in both Silicon-On-Insulator (SOI) and bulk CMOS technology. Which are valid for reverse biased p-n junctions. As in DTMOS source substrate junction is slightly forward biased, therefore due to presence of mobile charge carriers models based on depletion approximation are not appropriate for modeling of DTMOS and may introduce errors in DTMOS parameters like mobility, threshold voltage.

DTMOS technique is the best solution for reduction of threshold voltage (Vth). Therefore, an effective method for reducing power consumption is to reduce the power supply

voltage (Vdd). Reduction of power supply voltage (Vdd) depends on one of the factor that is threshold voltage. So one of the possible solutions is to implement CMOS transistors with dynamic Vth, which is the basic idea behind DTMOS technique. DTMOS transistor shows high threshold characteristic when it is in "off" condition to minimize the leakage current as well as, it behaves as a low threshold device in "on" condition at lower supply voltages for high current driving capability. This is one of the feature that makes DTMOS technique most suitable for low-voltage, low power applications.

1.1 DTMOS TECHNIQUE

From the past few years due to the extensive growth of market for portable devices such as cell phones, portable computers, other low power applications and also the design of analog circuits which requires low power, low voltage with high performance has become an important issue now a day's. One of the limitations for implementation of portable devices and design of other low power circuits at low voltage is the threshold voltage (Vth). For this reason reduction of threshold voltage is necessary for low-power, low-voltage operation. DTMOS technique is the best solution for reduction of threshold voltage (Vth). Therefore, an effective method for reducing power consumption is to reduce the power supply voltage (Vdd). Reduction of power supply voltage (Vdd) depends on one of the factor that is threshold voltage. So one of the possible solutions is to implement CMOS transistors with dynamic Vth, which is the basic idea behind DTMOS technique. DTMOS transistor shows high threshold characteristic when it is in "off" condition to minimize the leakage current as well as, it behaves as a low threshold device in "on" condition at lower supply voltages for high current driving capability. This is one of the feature that makes DTMOS technique most suitable for low-voltage, low power applications.

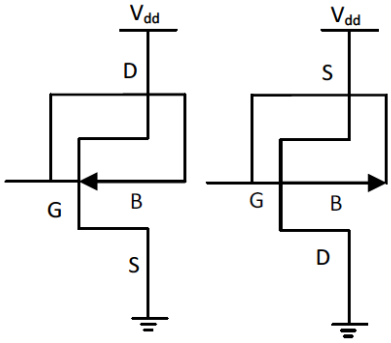


Fig.1.1 NMOS & PMOS transistors based on DTMOS circuit Topology

Dynamic Threshold voltage CMOS (DT-CMOS) with low on-resistance is designed to decrease conduction loss. The threshold voltage of DT-CMOS drops as the gate voltage increase, resulting in a much higher current handling capability than standard MOSFET. Low threshold voltage during the logic transition and high threshold voltage during the off state, the dynamic threshold circuit operates at high speed with low power. However, the dynamic threshold technique can only be used for low voltage (0.6 V and below) VLSI circuits. In a standard DTMOS logic gate, all transistor gates are tied to their substrates. The high speed operation is provided by forward bias to switching transistors, while low leakage is obtained by applying zero bias to other transistors. Specifically, the body-source junction is "forward biased" (at less than 0.6 V), forcing the threshold voltage to drop.

1.2 BCD ADDER

A BCD adder adds two BCD digits and produces a BCD digit A BCD cannot be greater than 9. The two given BCD numbers are to be added using the rules of binary addition. If sum is less than or equal to 9 and carry=0, then no correction is necessary. The sum is correct and in the true BCD form. But if sum is invalid BCD or carry=1, then the result is wrong and needs correction. The wrong result can be corrected by adding six (0110) to it.

The Boolean expression is,

$$Y = S_3S_2 + S_3S_1$$

The output of the combinational circuit should be 1 if C_{out} of adder-1 is high. Therefore Y is OR with C_{out} of adder 1 as shown in fig.4.1. The output of combinational circuit is connected to B_1B_2 inputs of adder-2 and $B_3 = B_1 = 0$ as they are connected to ground permanently. This make $B_3\,B_2\,B_1\,B_0 = 0110$ if Y' = 1. The sum output of adder-1 are applied to $A_3\,A_2\,A_1\,A_0$ of adder-2. The output of combinational circuit is to be used as final output carry and the carry output of adder-2 is too ignored.

OPERATION

Case 1: sum <= 9 and carry = 0

The output of combinational circuit Y' = 0. Hence $B_3\,B_2\,B_1\,B_0 = 0000$ for adder-2. Hence output of adder-2 is same as that of adder-1.

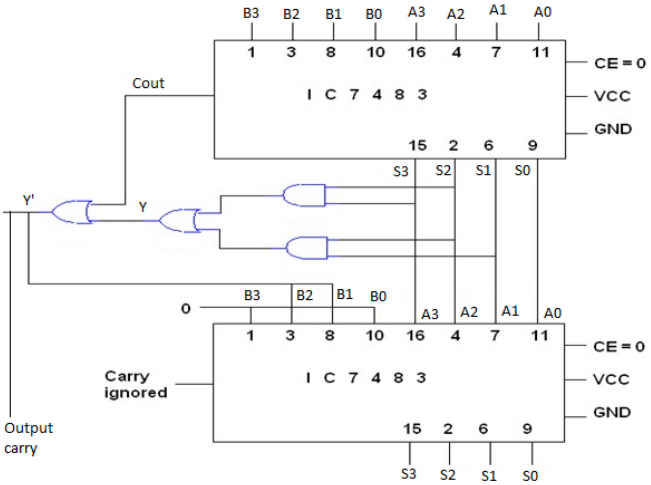


Fig.1.2 BCD Adder

Case 2: sum >= 9 and carry = 0

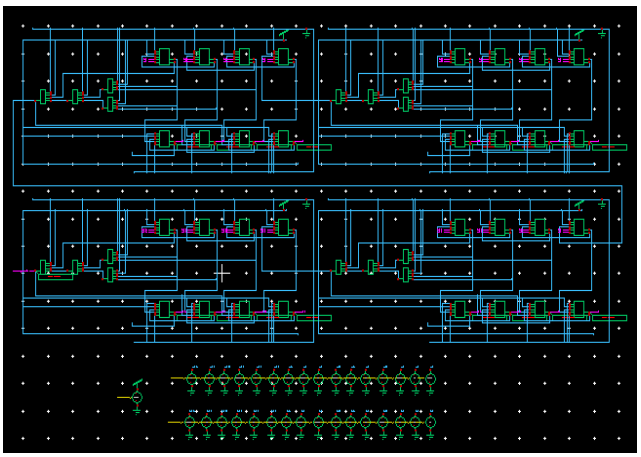
If $S_3\,S_2\,S_1\,S_0$ of adder-1 is greater than 9, then output Y' of combinational circuit becomes 1. Therefore $B_3\,B_2\,B_1\,B_0 = 0110$ (of adder-2). Hence six (0110) will be adder to the sum

output of adder-1.I get the corrected BCD result at the output of adder-2.

Case 2: sum <= 9 and carry = 1

As carry output of adder-1 is high, Y' = 1. Therefore B_3 B_2 B_1 B_0 = 0110 (of adder-2). Therefore 0110 will be added to sum output of adder-1. We get the corrected BCD result at the output of adder-2. Thus the sixteen bit BCD addition can be carried out using the binary adder.

2. DESIGN OF 16 BIT BCD ADDER



3. SIMULATION

The above design 16bit BCD adder has been simulated in Tanner EDA 22nm standard CMOS technology and DTMOS technology.

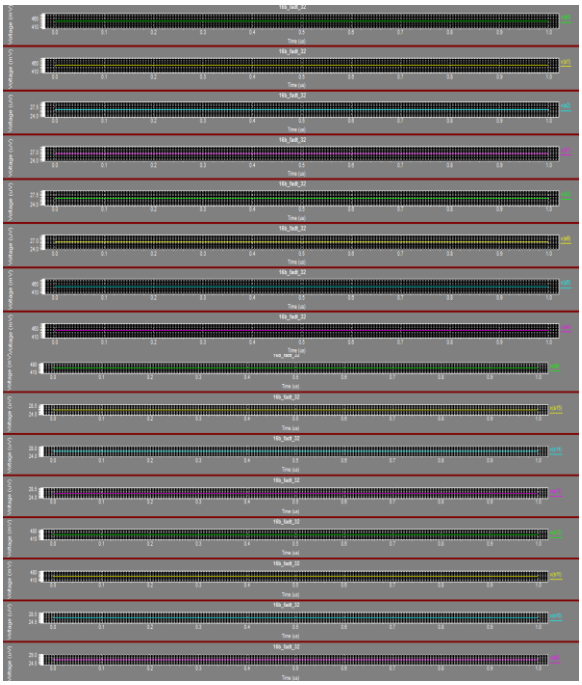


Fig3.1 Simulation results of 16bit BCD adder

4. RESULTS

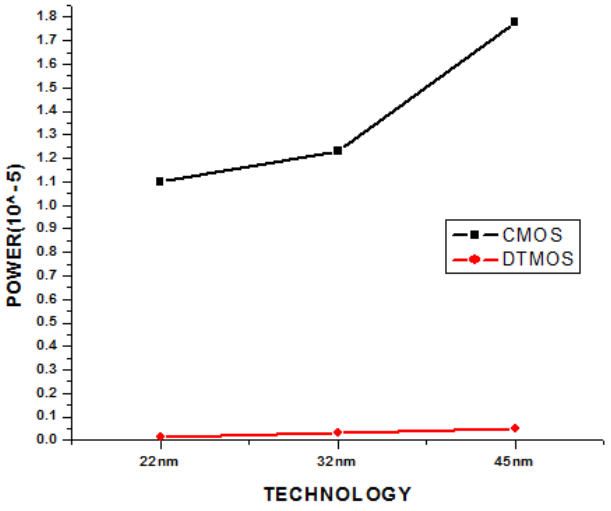
For CMOS

Tech	45nm	32nm	22nm
Power	1.78 e^{-5}	1.23 e^{-5}	1.10 e^{-5}
Delay	1.023 e^{-7}	1.016 e^{-7}	1 e^{-7}
Leakage current	4 e^{-6}	3.1 e^{-6}	2 e^{-6}
PDP	1.125 e^{-7}	1.016 e^{-7}	0.95 e^{-7}
Leakage power	4.4 e^{-6}	3.1 e^{-6}	1.9 e^{-6}

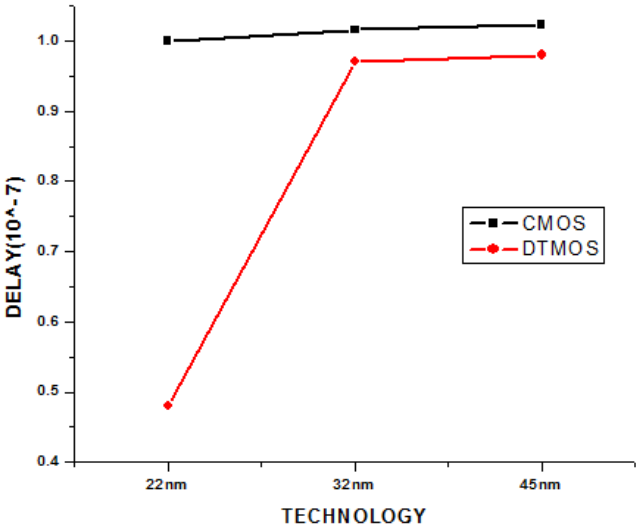
For DTMOS

Tech	45nm	32nm	22nm
Power	5.10 e^{-7}	3.12 e^{-7}	1.205 e^{-7}
Delay	9.86 e^{-8}	9.76 e^{-8}	4.84 e^{-8}
Leakage current	220 e^{-9}	140 e^{-9}	40 e^{-9}
PDP	4.93 e^{-8}	4.392 e^{-8}	1.69 e^{-8}
Leakage power	110 e^{-9}	63 e^{-9}	14 e^{-9}

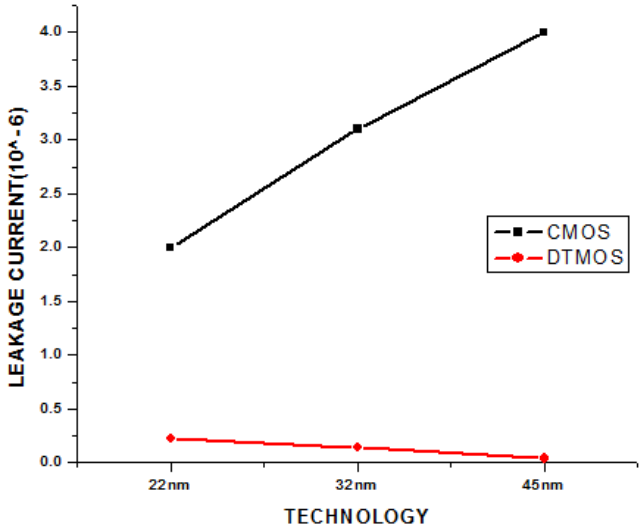
5. GRAPHS



Technology versus Power



Technology versus Delay



Technology versus Leakage current

6. CONCLUSIONS

The design of a low-power, low-voltage and high performance 16 bit BCD adder has been proposed in this paper. The BCD adder has been simulated in Tanner EDA at 45 nm, 32nm and 22nm CMOS technology. The BCD adder is designed for the purpose of low power applications. A DTMOS technique is used for the 16 bit BCD adder to achieve low power.

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