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DESIGNING OF SRAM USING LECTOR TECHNIQUE TO REDUCE LEAKAGE POWER

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Abstract: *In CMOS circuits, scaling of threshold voltage results in increase of sub-threshold leakage current. According to the International Roadmap of Semiconductor (ITRS), leakage is projected to grow exponentially during the next decade. LECTOR is a technique for designing CMOS gates in order to reduce the leakage current without affecting the dynamic power dissipation. From the results, it is observed Lector techniques produces lower power dissipation due to the ability of power gating. This paper presents the analysis comparison of leakage current, propagation delay, power dissipation, leakage power of the basic CMOS 8T, 12T Sram cell and cells implementing using LECTOR technique on 22nm, 32nm, 45nm technology using Tanner EDA tool. This technique results in reduction in Leakage current, power dissipation, leakage power up to 30%-50% and slight increase in delay.*

Key Words: ***Sub-threshold leakage current, dynamic power dissipation, Transistor stacking, Low power.***

1. INTRODUCTION

The increasing prominence of portable systems and need to limit the power consumption in very high density VLSI chips results in rapid and innovative growth of low power design. In several high performance designs, the leakage power consumption is becoming comparable to that of switching component. High power consumption leads to reduction in battery life in case of battery powered applications & also affects the reliability and cooling cost [2]. Thus the aim of low power design for battery powered devices is to enhance the service life of battery while fulfilling the performance requirements.

In digital CMOS circuits there are three main sources of power dissipation. The first is due to signal transition. The power dissipation due to transitions varies as the square of supply voltage. The second component of power dissipation comes from short circuit currents, which flows directly from the supply to the ground terminal at the time when n-sub network and p-sub network of a CMOS gate conduct simultaneously. The third source of power dissipation is leakage power dissipation which flows when the input(s) to and, therefore the outputs of a gate are not changing and it is called static dissipation. The leakage current comprised of six short channel mechanisms – reverse bias p-n junction leakage, sub threshold leakage, gate oxide leakage, gate current due to hot carrier injection, gate induced drain leakage, and channel punch-through current.

Among these components the two main contributors of leakage are reverse biased p-n junction current and subthershold current. The dynamic power and leakage power is given as follow:

Dynamic Power $P=C_L V^2_{DD} f_{clk}$

Leakage Power $P_{leakage=} V_{DD} I_{Leakage}$

Where CL is the total load capacitance, VDD is supply voltage, and fclk is the clock frequency. Thus lowering the supply voltage is the most effective way to achieve low power performance as the dynamic power varies as the square of supply voltage and the leakage power varies linearly with supply voltage. But reducing the supply voltage and keeping the threshold voltage at its original value results in drastic degradation in speed [2], because as the supply voltage is reduced the gate drive voltage (VDD-VT) reduces and thus the delay increases, since propagation delay in a CMOS gate is approximated as

$T_{d=} C_l V_{DD}/(V_{DD}-V_T)^{\alpha}$

Where CL is the total load capacitance, VDD is supply voltage , α is small positive constant used to that models the short channel effects. The value of α≈ 1.3 for short channel devices and α≈2 for long channel devices. To overcome the delay degradation, threshold voltage (VT) is to be reduced. Reduction in threshold voltage causes an exponential increase in sub-threshold leakage current. As one continues to scale down supply voltage and threshold voltage, the increased leakage power can dominate the dynamic switching power [3] [4].

There is work done on logic gates, 6T sram cell using Lector technique. Narender Hanchate et.al [1], LECTOR: A Technique for Leakage Reduction in CMOS Circuits. Experimental results indicate an average leakage reduction of 79.4% for MCNC'91 benchmark circuits. Experimental results simulated in HSPICE tool with 180 nm technology. Preeti varma et.al [2], Leakage Power and Delay Analysis of LECTOR Based CMOS Circuits. The HSPICE simulator is used to measure leakage power. Simulation is performed by taking 180-nm process parameters. From the experimental results it can be verified that an average saving of 66% for leakage power reduction with 16% increase in delay.

Siddesh Gaonkar et.al [3], Design of cmos inverter using lector technique to reduce the leakage power. Using cadence at 180nm CMOS technology total power consumed by the CMOS inverter without LECTOR with a load capacitor of 5pF is about1.632E-6.and with LECTOR is 1.168E-6. Prof. M. Zahid Alam et.al [4], New Approach to Low-Power & Leakage Current Reduction Technique for CMOS Circuit Design. After analyzing on cadence tool the results in terms of average power consumption, dynamic power consumption, static power consumption, delay and PDP,

It is observed that Lector techniques produces lower power dissipation than the other techniques due to the ability of power gating. The work have been done in before for logic gates and 6T sram cell. In this paper we are analyzing powers dissipation, delay, leakage current and leakage power for 8T and 12T sram cell using proposed technique.

1.1 Lector technique

For reduction in the leakage power, the assembling of transistors from VDD to ground is the notion behind the LECTOR technique [1] In this method, two leakage control transistors are positioned in between the pull-up and pull-down network, this implies either one of the LCTs will continuously drives in its near cut-off region, this arrangement is shown in figure 1.1.

Between two nodes N1 and N2, LCT's are introduced. The gate of the LCT's is controlled by the source of the other. Since LCTs are self-controlled there is no need of external circuit. These two LCTs increases the resistance between VDD and ground, and thereby shrink the leakage current. The topology of a LECTOR CMOS gate is shown in Figure 6.1. Two LCTs are introduced between nodes N1 and N2. The gate terminal of each LCT is controlled by the source of the other, hence termed as self-controlled stacked transistors. As LCTs are self-controlled, no external circuit is needed; thereby the limitation with the sleep transistor technique has been overcome. The introduction of LCTs increases the resistance of the path from Vdd to Gnd, thus reducing the leakage current. [1].

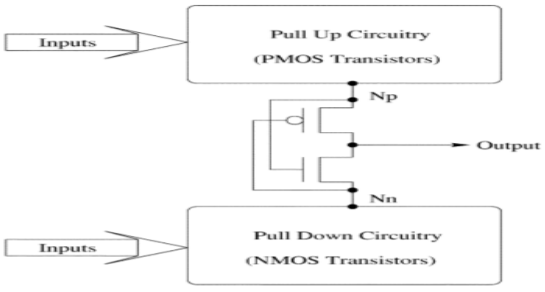


Fig 1.1: Generalized structure for leakage controlled gates

2 DESIGNING OF SRAM USING LECTOR TECHNIQUE

2.1 8T SRAM using Lector technique

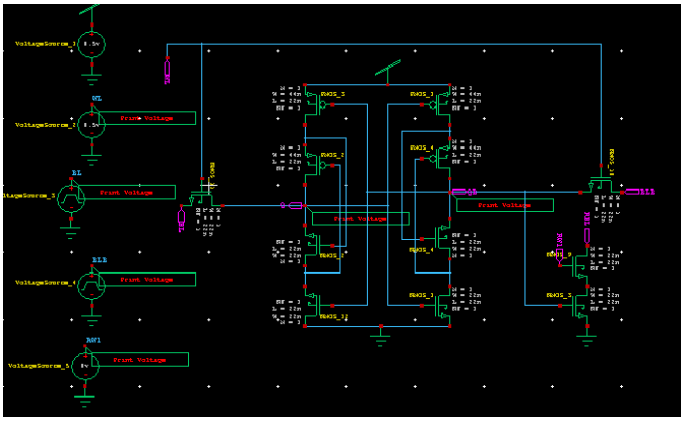


Fig 2.1: 8T SRAM write operation.

2.1.1 8T write operation:

For the write operation, in order to store logic =1 to the cell, BL is charged to Vdd and BLB is charged to ground and for writing logic =0 BL is charged to ground and BLB is charged to Vdd. The voltage on each of the internal load line will be a constant voltage for a particular memory data in an application, one of the two transistors of the leakage control configuration will remain in its cutoff state leading to a control over the leakage current. Then the NMOS access transistors are turn ON by switching the word line to Vdd. When the access transistors are turned ON, the values of the bit lines are written into Node Q and Node QB. The node which storing the logic =1 will not go to full Vdd because of voltage drops across the NMOS access transistor.

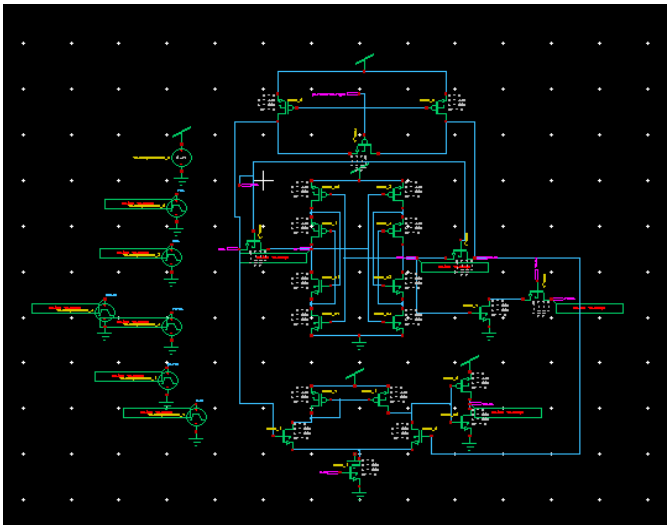


Fig2.2: 8TSRAM cell read operation.

2.1.2 8T read operation:

For the read operation, the RBL is charged to VDD. When the cell enters into the read mode, the RWL turns high and the WL signal turns low. The storage data is transferred to the bit line through M7 and M8. The dedicated read port temporarily decouples the read path from the storage nodes, enabling a nondestructive read operation since M5 is turned off. [7] Considering the logic 1 and 0 and the voltage on each of the internal load line will be a constant voltage for a particular memory data in an application, one of the two transistors of the leakage control configuration will remain in its cutoff state leading to a control over the leakage current.

Then operation of original Q stores =0 and QB Stores =1 and channel of the read connected to the ground. M8 has a path to the ground, so the value =0 store in Q will be transmitted to M8 Then let us assume the Q stores 1, then the QB stores 0, when the read word line is chosen, there is no path from GND to M8.

2.2 12T SRAM using LECTOR technique

Writ

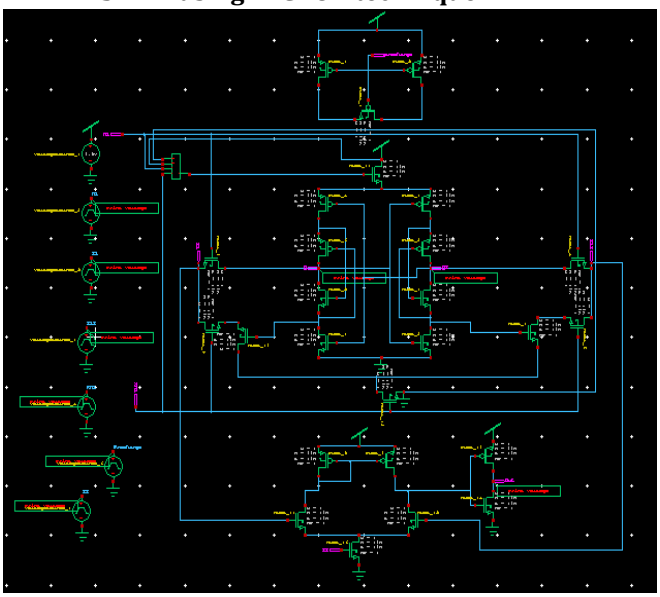


Fig: 2.3 12T SRAM read operation

2.2.1 12T Read operation:

The read operation is done only from QB storage node. In this mode RWL signal becomes one and BL and BBL pre-charge to one. When cell saves the one, (Q=1 and QB=0) the M10 becomes ON and reads the Q node by passing the current through M8 and M9. The voltage on each of the internal load line will be a constant voltage for a particular memory data in an application, one of the two transistors of the leakage control configuration will remain in its cutoff state leading to a control over the leakage current. On the other case, when zero is saved in cell (Q=0 and QB=1) the M8 becomes ON and BLB line discharges thorough M7 and M11.

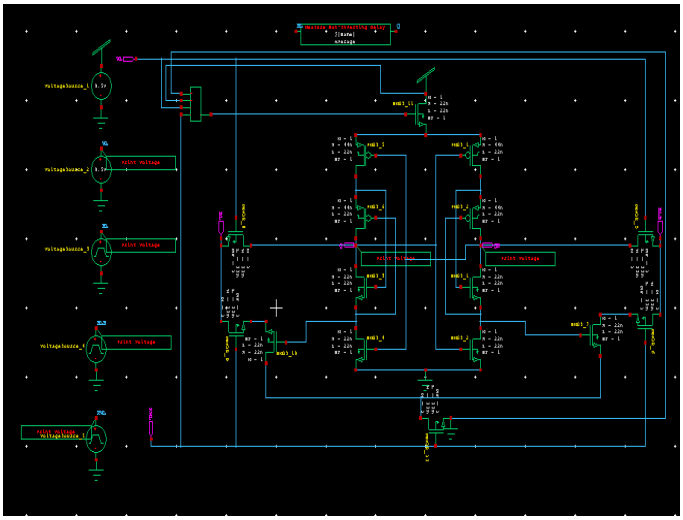


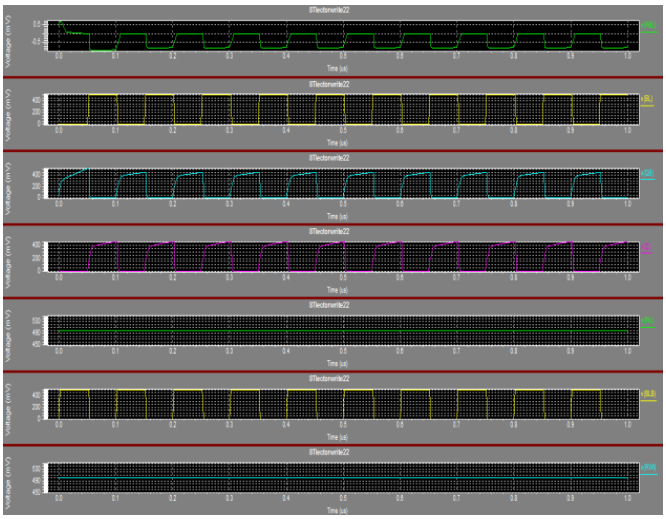
Fig: 2.4 12T SRAM write operation

2.2.2 12T write operation:

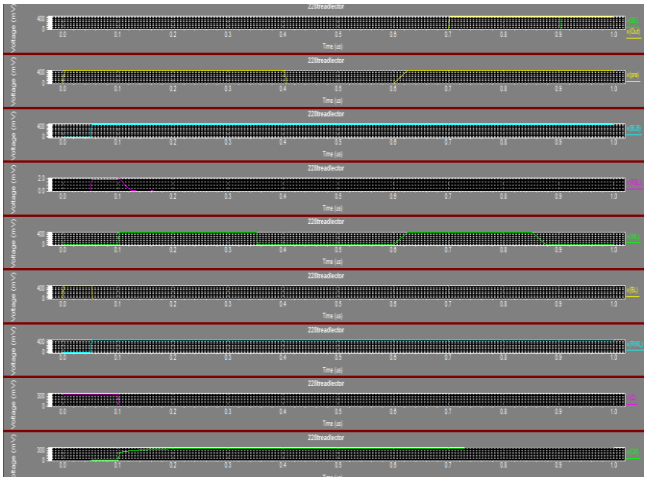
The write paths proposed architecture consist of two transistors (M5 and M6). In write mode, these transistors activate with WWL signal and write the value of BL and BLB on the storage nodes. The write operation can be performed at supply voltages as lower voltage. The voltage on each of the internal load line will be a constant voltage for a particular memory data in an application, one of the two transistors of the leakage control configuration will remain7 in its cutoff state leading to a control over the leakage current. Inability of access transistors to change the cell's value in write operation is called write failure.

3 SIMULATION RESULT:

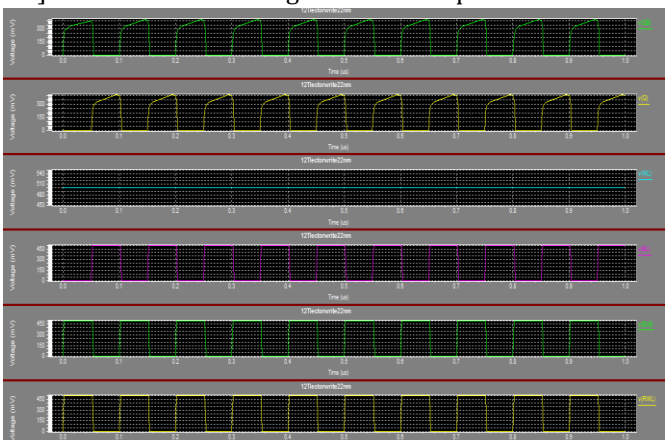
3.1] 8T write 22nm using lector technique



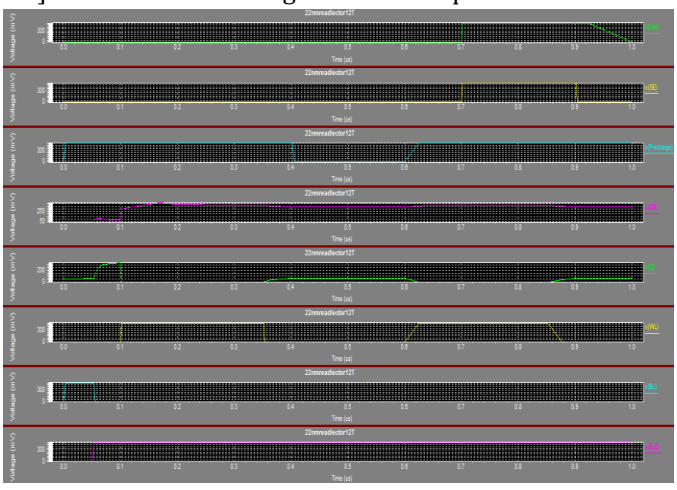
3.2] 8T read 22nm using lector technique



3.3]12T write 22nm using lector technique



3.4] 12T read 22nm using lector technique



4 RESULTS:

4.1] 8T write

		45nm	32nm	22nm
Power dissipation	Simple	2.009 e^{-7}	2.37 e^{-8}	2.03 e^{-8}
	Lector	9.82 e^{-8}	1.23 e^{-8}	1.25 e^{-8}
Leakage current	Simple	41 uA	25 uA	12.9 uA
	Lector	380 nA	330 nA	140.5 nA
Leakage power	Simple	2.009 e^{-7}	2.13 e^{-8}	1.61 e^{-9}
	Lector	8.83 e^{-8}	8.61 e^{-9}	6.25 e^{-8}
delay	Simple	5.27 e^{-8}	5.23 e^{-8}	1.23 e^{-9}
	Lector	5.36 e^{-8}	5.32 e^{-8}	2.12 e^{-9}

4.2] 8T read

		45nm	32nm	22nm
Power dissipation	Simple	4.53 e^{-6}	2.58 e^{-6}	7.10 e^{-7}
	Lector	1.82 e^{-6}	1.23 e^{-8}	5.76 e^{-9}
Leakage current	Simple	12 uA	2.5 uA	1.7 uA
	Lector	13.5 nA	5.2 nA	2.2 nA
Leakage power	Simple	4.53 e^{-6}	2.32 e^{-6}	4.97 e^{-7}
	Lector	1.63 e^{-6}	8.61 e^{-9}	2.88 e^{-9}
Delay	Simple	1.01 e^{-7}	1.006 e^{-7}	9.93 e^{-8}
	Lector	1.009 e^{-7}	1.013 e^{-7}	9.96 e^{-8}

4.3] 12 T write

		45nm	32nm	22nm
Power Dissipation	Simple	2.02 e^{-7}	1.05 e^{-7}	5.10 e^{-8}
	Lector	8.61 e^{-8}	4.36 e^{-8}	6.66 e^{-9}
Leakage current	Simple	27 uA	15 uA	3.3 uA
	Lector	7 nA	2 nA	25 pA
Leakage power	Simple	2.7e^{-5}	1.35 e^{-5}	2.31 e^{-6}
	Lector	6.3 e^{-9}	1.4 e^{-9}	1.25 e^{-11}
Delay	Simple	5.22 e^{-8}	5.13 e^{-8}	4.90 e^{-8}
	Lector	5.31 e^{-8}	5.24 e^{-8}	5.15 e^{-8}

4.4]12 T read

		45nm	32nm	22nm
Power dissipatio	Simple	5.69 e^{-6}	4.77 e^{-6}	7.52 e^{-7}
	Lector	2.46 e^{-6}	1.66 e^{-6}	2.79 e^{-9}
Leakage current	Simple	260 nA	37 nA	23 nA
	Lector	41 nA	380 pA	50 pA
Leakage power	Simple	5.69 e^{-6}	4.29 e^{-6}	5.26 e^{-7}
	Lector	2.23 e^{-6}	1.16 e^{-6}	5.39 e^{-9}
delay	Simple	1.021 e^{-7}	1.016 e^{-7}	9.92 e^{-8}
	Lector	1.029 e^{-7}	1.025 e^{-7}	9.95 e^{-8}

5 CONCLUSION:

In nanometer scale CMOS technology, sub-threshold leakage power is compatible to dynamic power consumption, and thus handling leakage power is a great challenge. This paper presents "LECTOR" to tackle the leakage problem. LECTOR uses two additional self controlled transistors. Like other leakage reduction techniques, such as sleepy stack, sleepy keeper, etc, LECTOR also achieves leakage power reduction but with the advantage of not affecting the dynamic power as this technique does not require any additional control and monitoring circuitry like in and also maintains exact logic state.

LECTOR technique can retain logic state, so it can be used for both generic logic circuits as well as memories, i.e., SRAM. When applied to Static RAM, the LECTOR technique achieves up to 30%-50% leakage reduction over the conventional circuit without affecting the dynamic power.

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