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A Novel Three Phase Asymmetric Multilevel Inverter with Series H-bridges

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Abstract- *A novel three phase asymmetric Multilevel Inverter with series H-bridges is proposed. The proposed topology is based on a cascaded connection of H-bridges to generate more levels at the output side of voltage by using different voltages of DC source voltages on both sides of the inverter. This topology is used to generate all positive, negative and zero levels by using a lower number of IGBT's, DC sources and controlling circuit parameters that leads to lower THD, reduction in installation space, cost of inverter is low, reduced radio frequency interface(RFI) and increasing the life of inverter also. It reduces not only switching network such as power electronic components, and also reduces the blocked voltages at each IGBT. An Asymmetric cascaded MLI uses different magnitudes of voltages that leads to the more number of levels at the output as compared to that of the Symmetric cascaded multi level inverter[MLI]. The performance of A novel three phase asymmetric MLI with series H-bridges have been verified by using three phase MLI of MATLAB/SIMULINK.*

Key Terms- **Three phase asymmetric, Cascaded multilevel inverter, H-bridges, radio frequency interference.**

I.INTRODUCTION

In today's world, Multi Level Inverters (MLI's) are more popular because of their huge advantages over than the conventional inverters. The main advantages of MLI's are lower voltage changing rate, lower amount of THD, lower amount of switching loss and better power quality. The cascaded MLI's (CMLI's) are gaining popularity because of easy control, easily identification of error circuits and modularity of the devices. CMLI's are categorized based upon their using DC sources are as follows,

1) Symmetric CMLI's and

2) Asymmetric CMLI's

Symmetric CMLI's are having same magnitude of applied voltages on both sides of the inverter. Asymmetric CMLI's are having different magnitudes of applied voltages on both sides of inverter. Asymmetric CMLI's are generate more number of output levels than the symmetric CMLI's [1],[2]. Symmetric CMLI's are having bidirectional switches includes driver circuit, two number of IGBT's and power diodes if that may leads the increasing of total cost of an inverter and installation space also be increased[3],[4]. Different symmetric CMLI's are on [5]. Asymmetric CMLI's are having unidirectional switches and bidirectional switches from voltage and current point of view. Unidirectional switches include of an IGBT with an antiparallel diode. Different Asymmetric CMLI's are on [6]. An Asymmetric cascaded MLI uses different magnitudes of voltages that leads to the more number of levels at the output as compared to that of the Symmetric cascaded MLI[7].

This topology is used to generate all positive, negative and zero levels by using a lower number of IGBT's, DC voltage sources and controlling circuit parameters that leads to lower THD, reduction in installation space, cost of inverter is low, reduction in radio frequency interface (RFI) and increasing the life of inverter also[8]. The proposed one is developed by using of a novel single-phase CMLI with series connection of the novel H-bridge basic units.

The basic H-bridge unit is

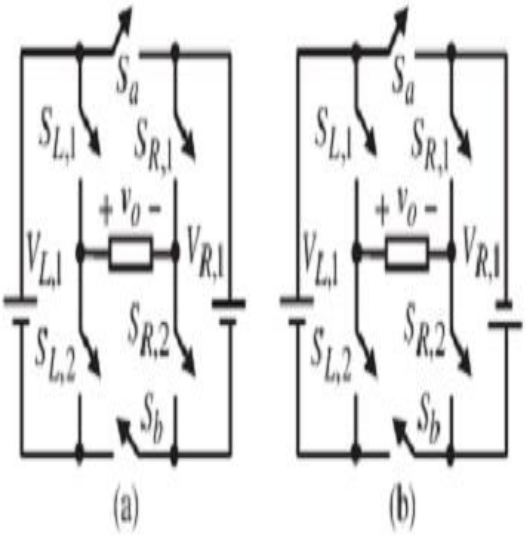

Fig 1:seven level H-bridge. (a) First Proposed Topology (b) Second Proposed Topology .

Table 1:OUTPUT SEQUENCE VOLTAGES OF A H-BRIDGE

STATE	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	Vo
1	0	1	1	0	0	1	$V_{R,1}$
2	1	0	0	1	0	1	$V_{L,1}$
3	1	0	1	0	0	1	$V_{R,1}+V_{L,1}$
4	1	0	1	0	1	0	0
	0	1	0	1	0	1	
5	1	0	0	1	1	0	$-V_{R,1}$
6	0	1	1	0	1	0	$-V_{L,1}$
7	0	1	0	1	1	0	$-(V_{R,1}+V_{L,1})$

Considering Table I, to generate all voltage levels (odd and even) in the proposed topology. From the table I, we observes the three positive levels, three negative levels and one zero level are generate by using single phase basic H-bridge. By cascading the two single phase H-bridges, we are generate 49 levels with a maximum amplitude of output voltage.

II. PROPOSED TOPOLOGY

The basic novel H-bridge is shown in Fig 1,it having of six unidirectional power switches named as $S_{L,1}$,$S_{L,2}$,S_A,S_B,$S_{R,1}$ and $S_{R,2}$. These power switches are able to generate seven levels, in the similar way the proposed one consists two H-bridges. The two H-bridges consists totally twelve IGBT's and four insulated DC sources. The twelve IGBT 's named as $S_{L,11}$, $S_{L,12}$, $S_{L,21}$, $S_{L,22}$, $S_{R,11}$, $S_{R,12}$, $S_{R,21}$, $S_{R,22}$, $S_{A,1}$, $S_{A,2}$, $S_{B,1}$and $S_{B,2}$.

The proposed topology for single-phase Asymmetric 49-level inverter is shown in Fig 2.

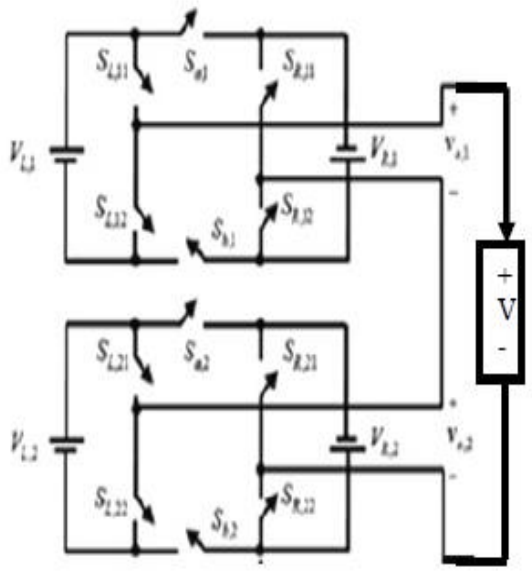

Fig 2: Asymmetric 49-Level Inverter

The power switches of each leg is activated simultaneously that means for each and every switching pattern, the switches $S_{L,1}$ or $S_{L,2}$, $S_{R,1}$ or $S_{R,2}$, S_A or S_B of a single H-bridge.

Magnitudes of DC voltages for a single H-bridge is

$$V_{R,1}=V_{DC} \quad (1)$$

$$V_{L,1}=2V_{DC} \quad (2)$$

The total output voltage is determined by the equation,

$$V_o(t)= V_{o,1}(t)+ V_{o,2}(t) \quad (3)$$

$V_{o,1}(t)$ is the peak voltage at the output of first H-bridge,

$$V_{o,1}(t)=V_{R,1}+V_{L,1}=3V_{DC} \quad (4)$$

$V_{o,2}(t)$ is the maximum voltage at the output of second H-bridge,

$$V_{o,2}(t)=7V_{R,1}+7V_{L,1}=21V_{DC} \quad (5)$$

Hence the total output voltage of proposed system is given by equation(6),

$$V_o(t)= V_{o,1}(t)+ V_{o,2}(t)=24V_{DC} \quad (6)$$

Then the output voltage from peak to peak is

$$V_{p\text{-}p}=2\ V_o(t) \quad (7)$$

The blocked voltages by all IGBT's in the first bridge is

$$V_{block,1}=4(V_{R,1}+V_{L,1}) \quad (8)$$

The maximum amount of blocked voltages in the proposed system is

$$V_{block}=4(V_{R,1}+V_{L,1}+V_{R,2}+V_{L,2}) \quad (9)$$

An Asymmetric CMI (ACMI) consists of unequal capacitor voltages. Rather than utilizing an identical DC link for each H-bridge converter, different DC links can be utilizes to synthesize a greater number of output voltage levels without any additional complexity to the existing topology. Each cell is supplied by an unequal DC voltage source. To focus the voltage levels among distinctive. DC links, a binary system can be effectively used,

i.e., $1V_{DC}$, $2V_{DC}$, $4V_{DC}$... $2(N\text{-}1)V_{DC}$, where N is the number of H-bridge converters in one phase leg.

III. PERFORMANCE OF A THREE-PHASE ASYMMETRIC INVERTER

Before going to proposed topology, let us examine single-phase asymmetric inverter, asymmetric inverter has four DC source voltages having ranges are $V_{R,1}$=10V, $V_{L,1}$=20V, $V_{R,2}$=70V and $V_{L,2}$=140V. Therefore the total maximum output voltage is V_{max}=240V. The three-phase inverter is developed by using three single-phase

inverters. Each single-phase inverter includes two asymmetric H-bridges with four different voltage sources such as $V_{L,1}$, $V_{R,1}$, $V_{L,2}$, and $V_{R,2}$.

IV. SIMULINK MODELS AND RESULTS

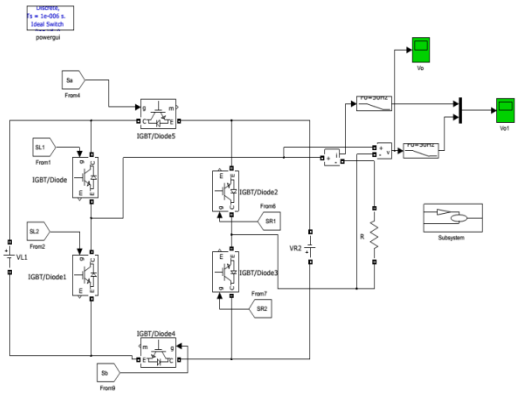

Fig 3: Seven Level Inverter

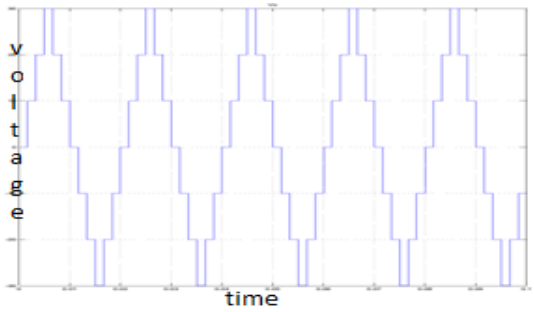

Fig 4: Seven Level Inverter Simulink Results

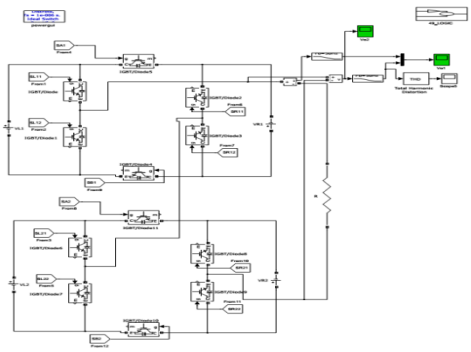

Fig 5: Asymmetric 49-Level Inverter

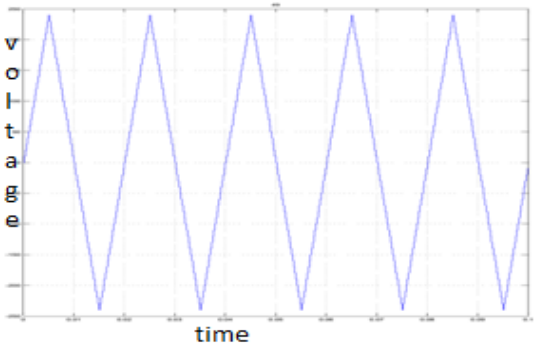

Fig 6: Output Voltage

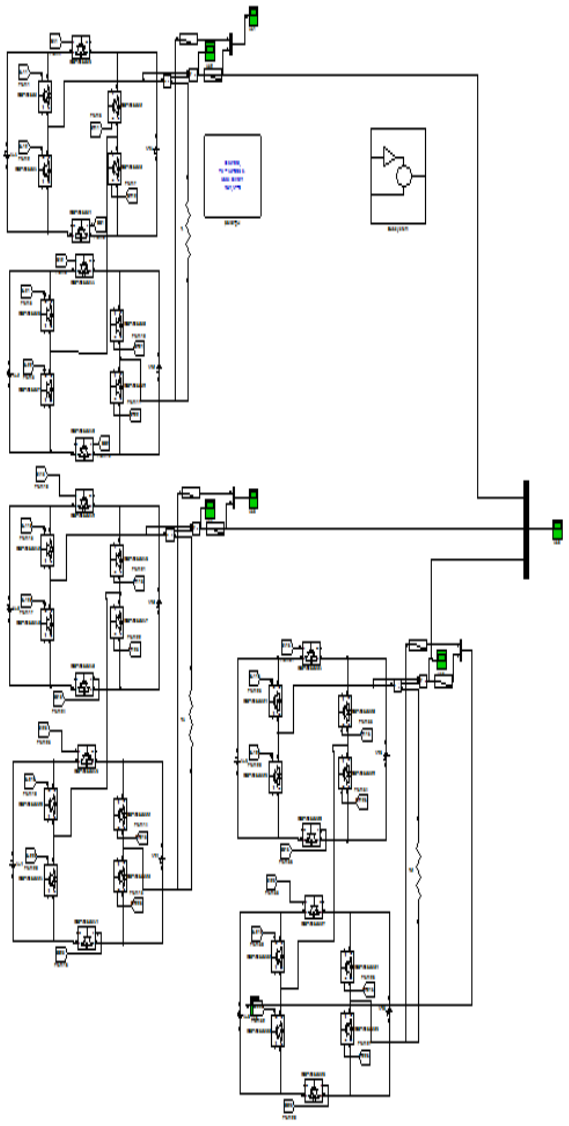

Fig 7: Three-Phase Asymmetric Multilevel Inverter

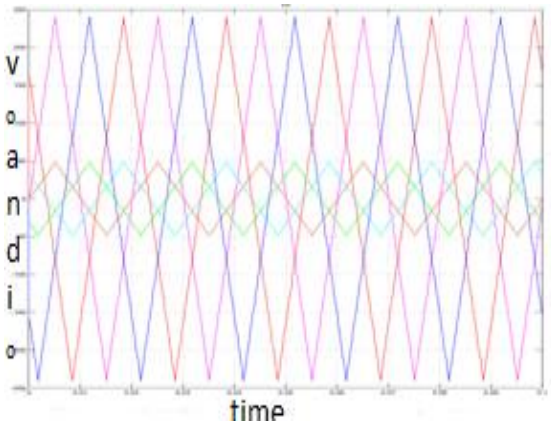

Fig 8: Three-Phase Current And Voltage

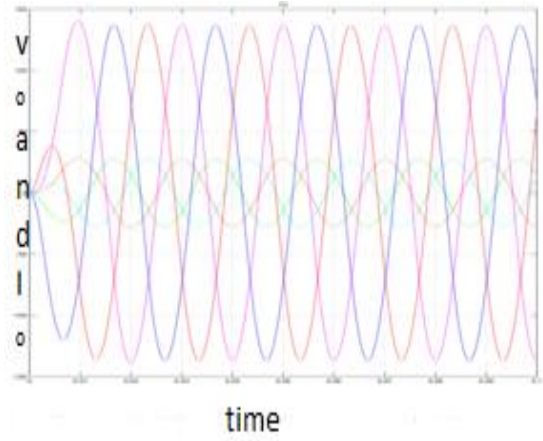

Fig 9:Three-Phase Filtered Current And Voltage

V.CONCLUSION

In this paper, two basic topologies have been proposed for multilevel inverters to generate seven voltage levels at the output. The basic topologies can be developed to any number of levels at the output where the 49-level and general topologies are consequently presented. In addition, a novel algorithm to determine the magnitude of the DC voltage sources has-been proposed. The proposed general topology was compared with the different kinds of presented topologies in literature from different points of view. According to the comparison results, the proposed topology requires a lesser number of IGBTs, power diodes, driver circuits, and DC voltage sources. Moreover, the magnitude of the blocking voltage of the switches is lower than that of conventional topologies. However, the proposed topology has a higher number of varieties of DC voltage sources in comparison with the others. The proposed novel three phase asymmetric multilevel inverter with series connection of H-bridge topology was verified through the matlab/Simulink platform through 49-level inverter.

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